VL4

INSTRUCTION MANUAL

VIKING LABS / HONEYWELL
370 BERNARDO AVENUE
MOUNTAIN VIEW, CA 94043

MODEL 8152
TIME CODE GENERATOR/
READER

SERIAL NO. 1220-1221

(D)

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SYSTRON DONNER CORPORATION

CONCORD INSTRUMENT DIVISION
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Instrument Division
10 Systron Drive
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STANDARD OPTIONS

Standard options installed in your unit are checked below. Circuit descriptions for these options are provided in Chapter 6. Special modifications, when included, are described in Chapter 7.

SERIAL NUMBER

OPTION		DESCRIPTION
A12A	☐	Slow Code, Type A
A12B	☐	Slow Code, Type B
A16	☐	Control Bit Insertion
A16C	☐	Control Bit Translation
A16D	☐	Control Bit Translation & LED Display
A19	☐	Group Parallel BCD Outputs
A21	☐	Computer Read Command
B11	☑	Crystal Oscillator with stability (±4 parts in 10^9)
B13	☐	Crystal Oscillator with stability (±4 parts in 10^9)
B14	☐	Crystal Oscillator, Zero Warmup (±5 parts in 10^7)
B17	☐	Flywheel Oscillator
C11	☐	IRIG A (10 kHz) Code
C12A	☐	Binary Seconds (17-Bits in Code)
C12B	☐	Binary Seconds (TOD) Parallel Output
C12Q	☐	IRIG B (1 kHz) Code
C17	☐	NASA 28-Bit (100 Hz) Code
C18	☐	NASA 36-Bit (1 kHz) Code
C26	☐	XR3 (250 Hz) Code
C26A	☐	XR3 (1 kHz) Code
C31	☐	IRIG G (100 kHz) Code
C40	☐	IRIG A,B,C Switch Selectable
C41	☐	IRIG A,B Switch Selectable
C47	☐	XR3 (250 Hz/1 kHz) Switch Selectable
C48	☐	IRIG H (100 Hz) Code
C48A	☐	IRIG H (1 kHz)
D12	☐	Buffers, Positive Level
D13	☐	Buffers, Negative Level
D14	☐	Buffer Storage
D15	☐	Parallel BCD Output

OPTION		DESCRIPTION
E13	☑	Days/ID Number
E14	☐	Parallel BCD Output, Milliseconds
E17	☐	Simultaneous Generate/Read (Hours,Minutes,Seconds)
E17A	☐	Simultaneous Generate/Read (Days,Hours,Minutes,Seconds)
L12	☐	48 Hz to 440 Hz Operation
L13	☐	AC/DC Power Supply
P11	☐	Mode, Preset & Reset Switches (Single line control)
P12	☐	Time Preset in BCD Format (Hours,Minutes,Seconds - Single line control)
P12A	☐	Time Preset in BCD Format (Days,Hours,Minutes,Seconds - Single line control)
P14	☐	Code Selector Switch for Option C40 (Single line control)
P20	☐	Slow Code Rate Selector Switch for Option A12 (Single line control)
S11	☐	External Synchronization
S11A	☑	WWV Synchronization
S13	☐	Analog Filters
S14	☐	Analog Filters with Remote Select
	☑	Special Modifications (See Chapter 7)

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8152 Time Code Generator/Reader combines the features of both a generator and a reader.

As a Time Code Generator, the Model 8152 is a precise digital clock which displays time and generates a serial time code. This time code may be used in applications where real or elapsed time must be maintained for control, recording or display.

As a Time Code Reader, the Model 8152 decodes an incoming serial modulated time code. Time information, stripped from the input code, is displayed and fed, in parallel BCD form, to a rear panel connector. The Time Code Reader incorporates extended range AGC, error bypass, and digital filtering for reliable decoding of the incoming time code.

The basic unit generates or reads a modified IRIG B time code on a 1 kHz carrier. Time is displayed in hours, minutes and seconds. Front panel thumbwheel switches are provided for entering Generator preset (Start) time in hours, minutes and seconds. Four pulse rates (1 pps, 10 pps, 100 pps and 1 kpps) are supplied as outputs.

Other time codes from the IRIG, NASA and XR3 code families may be substituted for IRIG B as options. The unit can be expanded to include Days/ID Number and to provide parallel BCD outputs representing Days/ID and/or Milliseconds. Other options are also available. (Refer to the standard option list at the front of this manual.)

The Model 8152 is constructed with highly reliable semiconductors and monolithic IC,s assembled on printed-circuit, plug-in modules for ease of maintenance.

TABLE 1-1 SPECIFICATIONS

Time Base (GENerate Mode)	Crystal-controlled 1 MHz oscillator with an aging rate of 1 part in 10^7 per day and an over-all stability of 1 part in 10^5 per day from 0° to 60°C. Provisions are included for the use of an external 1 MHz time base.
Display (GENerate and READ Modes)	A 6-digit, in-line, in-plane display indicates time-of-day in hours, minutes and seconds. Days option adds 3-digits. Numeral height is 0.55" (14 mm). Colons are provided between seconds and minutes, minutes and hours, and hours and days.
Code Format (GENerate and READ Modes)	Modified IRIG B format, in terms of BCD hours, minutes and seconds (Days/ID optional). Other IRIG, NASA or XR3 code formats are also available as options.

TABLE 1-1 SPECIFICATIONS (Cont'd)

INPUTS:	
External Time Base (GENerate Mode)	Accepts a 1 MHz (nominal) input at 1V p-p (nominal) into 1 kΩ via a rear panel BNC connector, selected by a rear panel INT/EXT selector switch.
Elapsed Time Command (GENerate Mode)	A +5V level (or open circuit) to enable or a ground condition to inhibit time advance via rear panel connector, Amphenol 57-40140.
Update Inhibit (GENerate or READ mode)	A +5V level (or open circuit) enables update. A ground condition delays update. Update may be delayed up to 0.5 ms without losing a count via rear panel connector, Amphenol 57-40140.
Modulate Code, External (READ Mode)	The input modulated code, via a rear panel BNC connector, may have a carrier frequency from 30 Hz to greater than 500 kHz, input levels from 50 mV to 50V p-p, and modulation rations from 2:1 to 6:1. Input impedance in 100 kΩ minimum.
OUTPUTS:	
Modulated Code (GENerate Mode)	The modulated code is generated on a 1 kHz carrier with an adjustable amplitude from a low impedance 15 mA source and an adjustable modulation ratio (Mark-to-Space) from 2:1 to 6:1. Connector is rear panel BNC type. The Code Format is modified IRIG B with BCD hours, minutes and seconds.
DC Level Shift Code (GENerate and READ Modes)	The DC Level Shift code is generated with an adjustable amplitude from 0 to 10V into a minimum 600Ω load. Connector is rear panel BNC type.
Pulse Rates (GENerate and READ Modes)	Simultaneous rates of 1 pps, 10 pps, 100 pps and 1000 pps are provided with leading edge "on time". Levels are 0 to +5V (nominal) from a 6 kΩ source (DTL). Connector is rear panel Amphenol 57-40140.
Parallel BCD (GENerate and READ Modes)	Updated time is provided as 24 parallel BCD bits (20 active) representing hours, minutes and seconds. Days/ID option adds 12 bits. Code: 8-4-2-1. Logic: "1" = 5 ±0.5V behind 6 kΩ. "0" = 0 ±0.5V, 12 mA sink. Connector is rear panel Amphenol 57-04500.

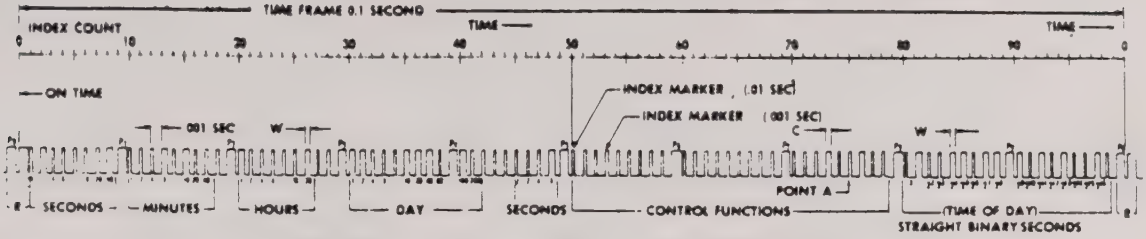
TABLE 1-1 SPECIFICATIONS (Cont'd)

START (PRESET) TIME SET:	A group of thumbwheel switches is used for selecting the initial Start (Preset) time for the Time Code Generator.
ENVIRONMENT:	
Operating	0°C to +60°C at up to 95% relative humidity.
Storage	-55°C to +85°C.
POWER:	115/230V ±10%, 48 to 62 Hz at less than 60W.
PACKAGE:	3-1/2" (8.9 cm) high by 19" (48.3 cm) wide by 17" (43.1 cm) deep. Removable rack flanges. Chassis drilled for Jonathan 120 QD series slides. Weight approximately 25 lbs (11 kg) net, 35 lbs (16 kg) shipping.

FIGURE 1.1 IRIG TIME CODE FORMATS

FORMAT A

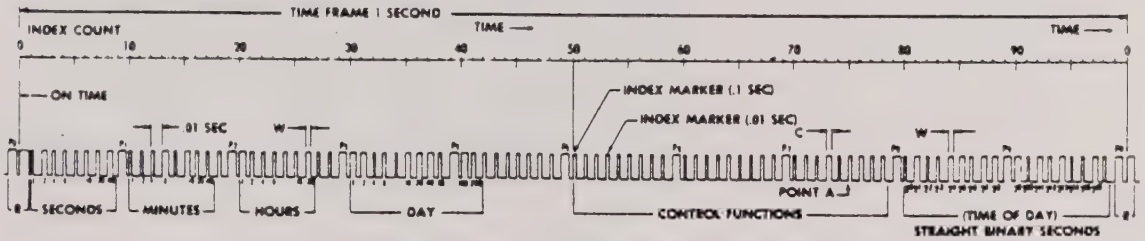
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A 21:18:42 . 8 . 07 . 005 21 HR. 18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

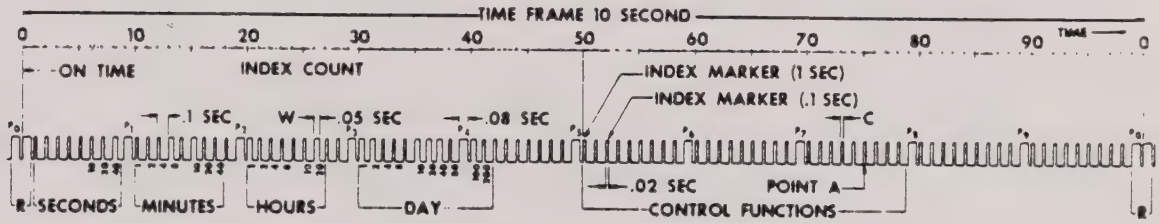
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A - 21:18:42 - .7 - .05 - 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

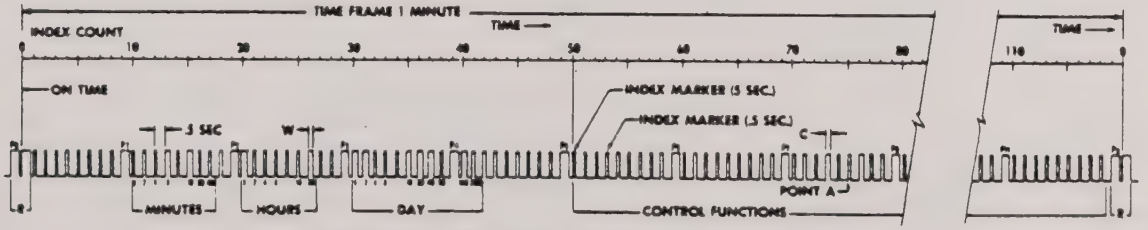
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A - 21:18:48 - 7 - .5 - 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

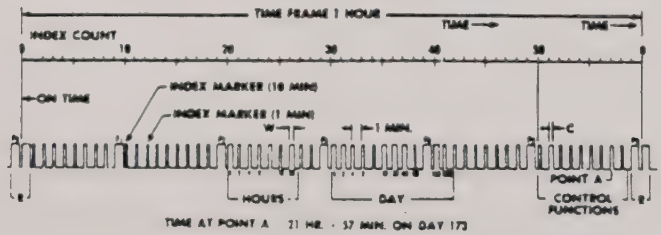
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



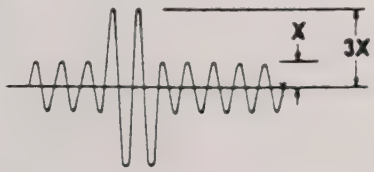
TIME AT POINT A - 21:18 - 37.5 SEC. - 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

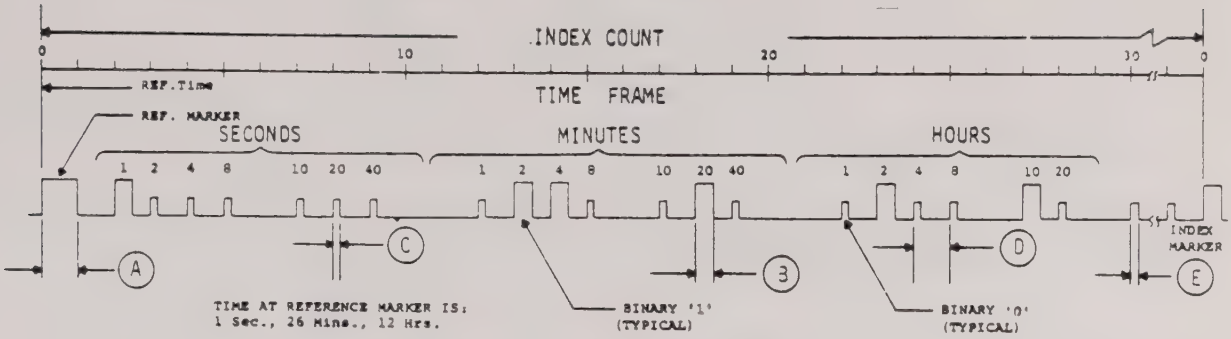


TIME AT POINT A - 21 HR. - 37 MIN. ON DAY 173



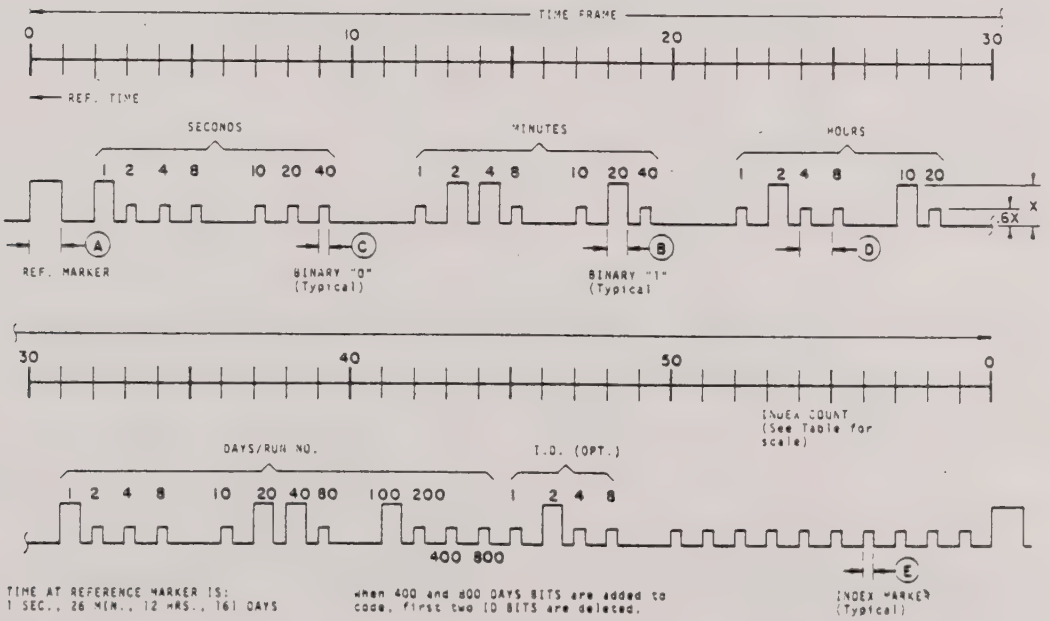
TYPICAL MODULATED SIGNAL

FIGURE 1.2 SLOW CODE - TYPE 'A'



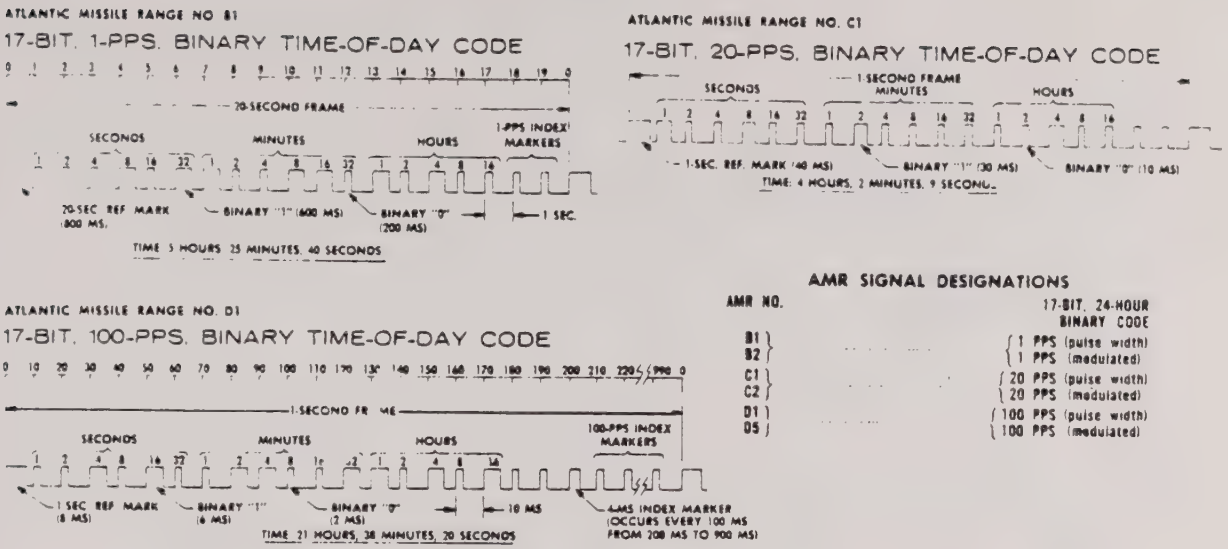
	RATE	TIME FRAME	O-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec.	1 Sec.	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs.	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1/10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1/20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1/2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

FIGURE 1.3 SLOW CODE - TYPE 'B'



Pulse Rate	Time Frame	O-Period	A-width	B-width	C-width	E-width	Number of Pulses in Time Frame
1. 50	1 SEC	20 ms	20 ms	10 ms	4 ms	4 ms	50
2. 10	5 SEC	100 ms	100 ms	50 ms	20 ms	20 ms	50
3. 5	10 SEC	200 ms	200 ms	100 ms	40 ms	40 ms	50
4 2	30 SEC	1/2 SEC	1/2 SEC	250 ms	100 ms	100 ms	60
5 1	60 SEC	1 SEC	1 SEC	1/2 SEC	200 ms	200 ms	60
6 1/2	5 MIN	5 SEC	5 SEC	2-1/2 SEC	1 SEC	1 SEC	60
7 1/10	10 MIN	10 SEC	10 SEC	5 SEC	2 SEC	2 SEC	60
8 2 ppm	30 MIN	30 SEC	30 SEC	10 SEC	6 SEC	6 SEC	60
9 1 ppm	60 MIN	60 SEC	60 SEC	30 SEC	12 SEC	12 SEC	60

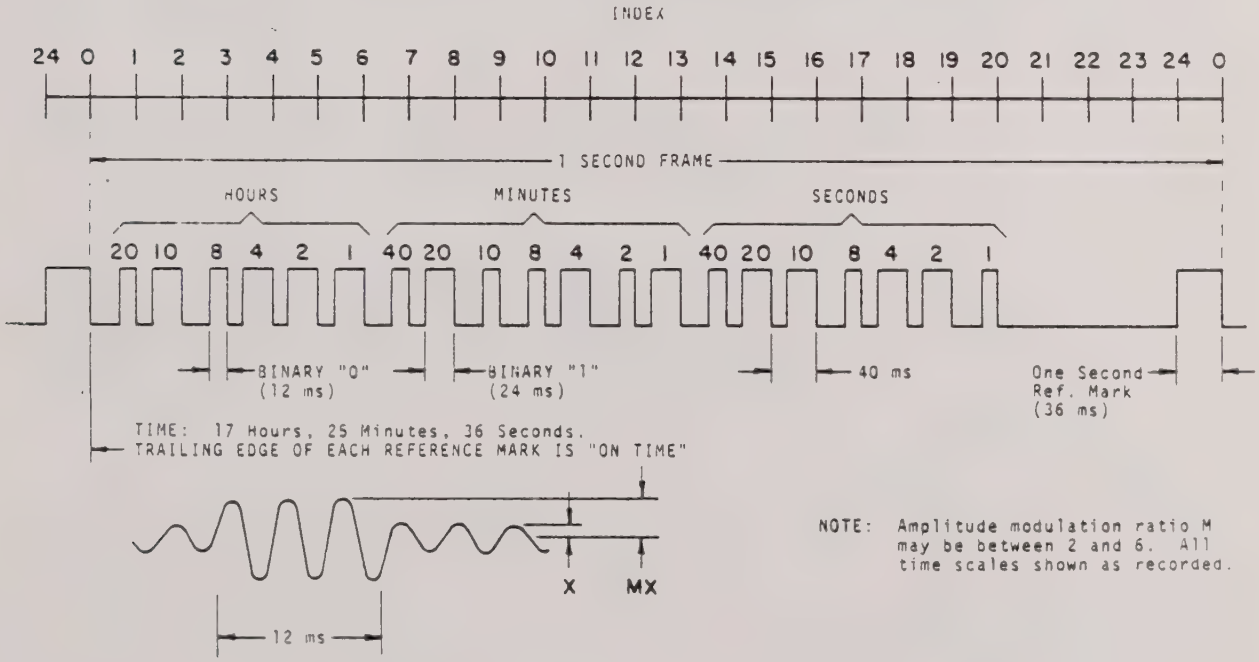
FIGURE 1.4 AMR TIME CODE FORMATS



AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1	1 PPS (pulse width)
B2	1 PPS (modulated)
C1	20 PPS (pulse width)
C2	20 PPS (modulated)
D1	100 PPS (pulse width)
D5	100 PPS (modulated)

FIGURE 1.5 XR3 TIME CODE FORMAT


INDEX
24 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 0
1 SECOND FRAME
HOURS
MINUTES
SECONDS
20 10 8 4 2 1 40 20 10 8 4 2 1 40 20 10 8 4 2 1
BINARY "0" (12 ms)
BINARY "1" (24 ms)
40 ms
One Second Ref. Mark (36 ms)
TIME: 17 Hours, 25 Minutes, 36 Seconds.
TRAILING EDGE OF EACH REFERENCE MARK IS "ON TIME"
X
MX
12 ms

NOTE: Amplitude modulation ratio M may be between 2 and 6. All time scales shown as recorded.

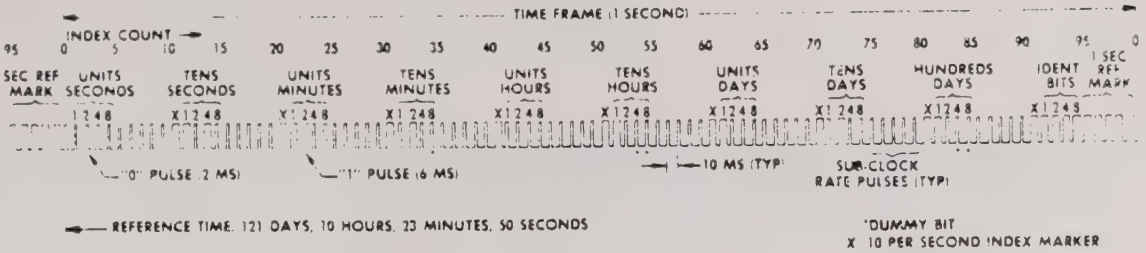
TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

FIGURE 1.6 NASA TIME CODE FORMATS

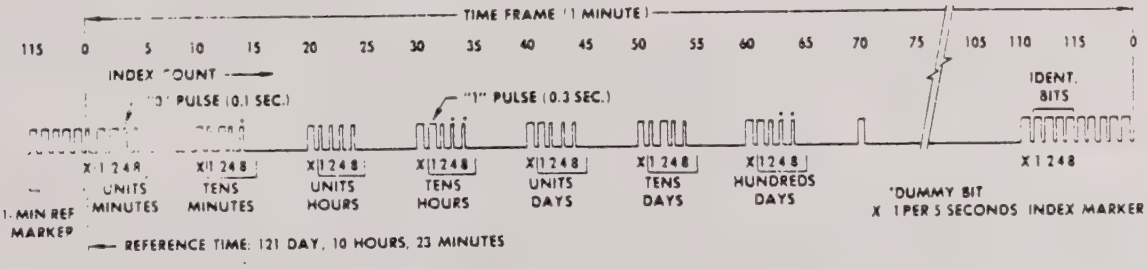
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES



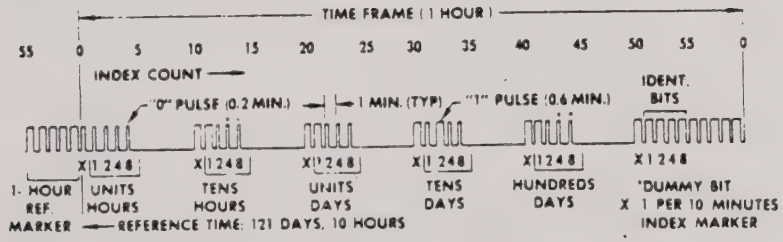
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB CLOCK RATE PULSES INHIBITED

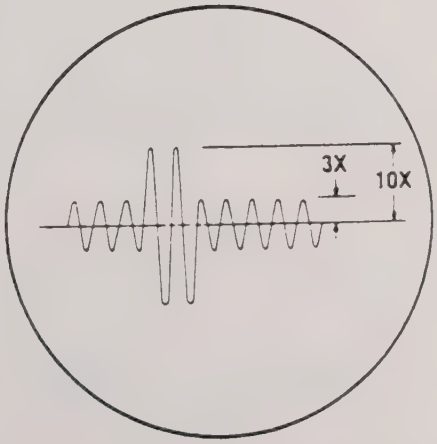


20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

CHAPTER 2

INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found refer to the warranty at the front of this manual and to Section 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.
2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb.sq.in. bursting strength) or wooden box to house the instrument.
3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.
4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".
5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER AND COOLING REQUIREMENTS

The Model 8152, unless otherwise specified, is supplied to operate from a 115V ±10%, 48 to 62 Hz source.

To adapt the instrument for 230V operation, push the rear panel SELECTOR switch, S101, to the "230" position and change Fuse F1, from 2A Slo-Blo to 1A Slo-Blo.

2.4 INITIAL ADJUSTMENT

To apply primary power to the Model 8152, it is only necessary to turn the Mode switch to PWR OFF, install the power cord (supplied), and turn the switch to GENerate.

2.4.1 Generator

The EXT-INT switch on the rear panel must be in the INT position to utilize the internal 1 MHz oscillator. If use of an external 1 MHz source is desired, the switch must be in the EXT position.

The Modulated Code Amplitude Adjustment Control on the Modulator Card (A20), denoted as MOD, must be adjusted to the input voltage required by the particular tape transport in use (1V p-p is standard). Voltage may be observed at the MOD JACK or at the MOD test point on Modulator Card (A20).

The Modulation Ratio Control (marked as RATIO) has been factory adjusted for a 3:1 modulation ratio and should not require further adjustment. If adjustment should become necessary, the RATIO control on Card A20 may be adjusted as desired.

If the Level Shift output is also to be used, potentiometer R19, on Modulator Card (A20), marked as DC, may be adjusted for the desired output level. Potentiometer R19 will adjust the Level Shift output from ground to +10V dc.

2.4.2 Reader

Turn the Mode switch to READ and introduce the appropriate code via connector J8. The unit should translate and display the time information contained in the code, provided the input code is within specifications. No adjustment of the AGC (AGC/Cycle Detector Card, A10) should be necessary.

2.5 INSTALLATION

The Model 8152 is normally supplied with hardware for rack-mount installation. For convenience, the unit has been drilled for 20" Jonathan 120 QD series slides. When slides are used, the rear support brackets are removed.

NOTE

Under no condition should air flow through the outlet hole in the rear of the unit be obstructed.

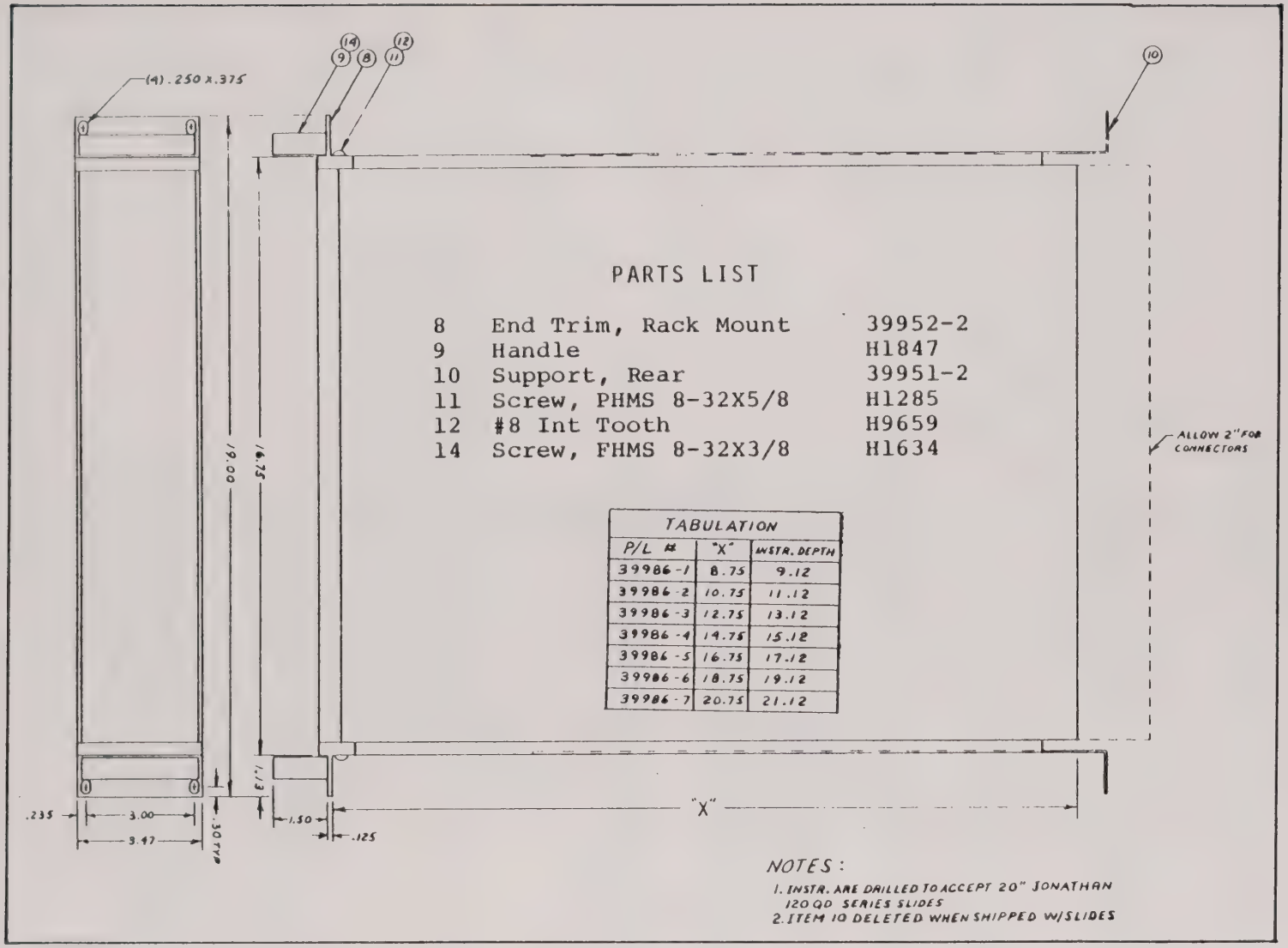


FIGURE 2-1 3-1/2" FULL RACK ASSEMBLY #039968-4-5 Rev A

CHAPTER 3

OPERATION

3.1 GENERAL

The Model 8152 is ready to operate immediately after turning on the power. Preliminary adjustments or calibration are not normally required. It is advisable that the following description on use of the instrument controls and indicators be read before operating the unit.

3.2 CONTROLS, INDICATORS AND CONNECTORS

3.2.1 Front Panel

1) Mode Selector: (Rotary Switch S3) — Controls main power and selects mode of operation.

PWR OFF:	Removes power to the unit.
STOP:	Arms PRESET/RESET switch. Stops time base counters. No outputs generated.
HOLD:	Stops the count in the display register. Latest count is displayed. Arms PRESET/RESET switch.
GENerate:	Permits normal update of the display register and generation of the serial time code. Arms PRESET/RESET switch for optional Days/ID only.

NOTE

When the mode selection switch is moved from STOP to HOLD, the code generation remains inhibited. when moved from GENerate to HOLD, code generation is normal, except that each frame will contain the same time information, since update does not take place in HOLD.

READ OE:	Places the unit in a Read mode condition which allows time information to be stripped from the input code and loaded into the display register.
READ 3E:	Places the unit in a Read mode condition such that transfer of time information into the display register is inhibited for up to three frames if an error is detected in forward.

2) PRESET/RESET:
(Momentary Toggle Switch, S4)

Armed in STOP, HOLD and GEN positions of Mode switch. PRESET Loads contents of Preset thumbwheel switches into display register. RESET forces display register contents to zero. (TOD not affected in GEN.)

NOTE

If the Days/ID Option is included, the Days/ID section of the display register can be independently preset or reset in the GENerate position of the Mode switch.

3) PRESET:
(Thumbwheel Switches; S6-S11 for TOD, S12-S14 for Days/ID)

Used to store start time for entry into the display register by PRESET/RESET

4) TAPE DIRECTION:
(Toggle Switch, S35)

NORMal position conditions unit to read a forward code. The REVerse position permits a reverse code to be read.

5)] DISPLAY:

A 6-digit, in-line, planar readout which indicates TOD in hours, minutes and seconds. Days/ID Option adds 3-digits.

6) TAPE ERROR:
(LED, DSI)

Indicates a discrepancy between the input code and the contents of the display register.

3.2.2 Rear Panel

1) BCD OUT/SEARCH CONTROL:
(50-pin connector, J3)

BCD Output of display register contents plus search control signals.

2) PULSE RATE:
(14-pin connector, J4)

Pulse rate and control lines.

3) CODE IN:
(BNC connector, J8)

Modulated Code input to Reader.

4) CODE OUT:
(BNC connector, J9)

Modulated serial time code output.

5) DC CODE:
(BNC connector, J10)

Serial level shift time code output.

6) EXT/INT 1 MHz:
(BNC connector, J12)

External 1 MHz Time Base input.

7) AC POWER:
(AC connector, J101)

Mates with ac line cord.

8) EXT/INT 1 MHz:
(Slide switch, S1)

Selects external or internal 1 MHz Time Base.

9) 115/230V Power Select:
(Slide switch, S101)

Adapts power transformer for 115 or 230 volt operation.

10)	BCD MS, Optional: (14-pin connector, J6)	BCD milliseconds outputs.
11)	Remote, Optional: (36-pin connector, J7)	Reserved for options.
12)	SLOW CODE, Optional: (BNC connector, J11)	Slow time code output.
13)	ID UPDATE, Optional: BNC connector, J13)	ID Update input (part of Days/ID Option).
14)	WWV IN, Optional: (BNC connector, J14)	WWV input to instrument.
15)	EXT START, Optional: (BNC connector, J15)	EXTernal start input to instrument.
16)	365-366-ID, Optional: (Slide switch, S33)	Leap Year/ID selector switch. (Part of Days/ID Option.)

CHAPTER 4
MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your nearest sales representative; or Sales Manager:

SYSTRON-DONNER CORPORATION
INSTRUMENT DIVISION
10 Systron Drive
Concord, California 94518
Phone: (415) 676-5000
TWX: 910-481-9479
Cable: SYSTRONDONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.

2) Make a through visual inspection of all wiring and cables. Check for frayed, loose or burned wires.

3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physcial damage. When a printed-circuit board contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure (Section 4.4). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component).

3) Apply heat (40-50 W soldering iron) sparingly to each of the cut pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component).

4) Form the tinned leads of the replacement part and insert in the printed-circuit holes; solder, then trim leads to extend 1/16-inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16-inch diameter).

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the solder connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol to freon-type solvents.

4.4 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the service engineer to isolate the trouble to a particular circuit card or subsection.

When the trouble is isolated, the functional description in Chapter 5 and Optional information in Chapter 6 will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8152.

TABLE 4.1 TEST EQUIPMENT FOR MODEL 8152

Model	Manufacturer	Minimum Specifications
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth triggered sweeps from 0.1 µs/cm to 5 sec/cm. Vertical sensitivity from 0.5 V/cm to 20 V/cm.
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7004A	Systron-Donner Corp.	DMM 10 MΩ input impedance, ±0.1% accuracy.
200AB	Hewlett Packard	Audio Oscillator, 20 Hz to 40 kHz coverage.
6250	Systron-Donner Corp	Frequency Counter, 0 Hz to 50 MHz, 3 parts/10^7 per week.

In addition to the equipment listed above, a suitable source of time code input signals with known characteristics is required. This may be a Time Code Generator or a prerecorded tape and tape playback equipment.

4.4.2 Power Supply Calibration Procedure (Dwg. #041810-7-9)

Check that fuse F1 is the proper size for the input voltage selected:

2A, 115 V

1A, 230 V

With an input of 115 V ac (230 V if so equipped) ±5%, 50/60 Hz. Check the following at the Power Supply P.C. Board, edge connector, P103.

1) +210 V ±25% at pins V, 18 (GND 20, X)
2) +21 V ±20% at pins S, 15 (GND BLACK TEST POINT)
3) +9 V ±20% at pins Y, 21 (GND BLACK TEST POINT)
4) -9 V ±20% at pin 2 (GND BLACK TEST POINT)
5) -21 V ±20% at pin 4 (GND BLACK TEST POINT)

Measure the +15 V supply on the BLUE (GND BLACK) Test Point and adjust R5 (15 V ADJ) for + 15 V ±0.3 V.

Measure the -15 V supply on the VIOLET Test Point and verify that it is within ±0.3 V of -15 V. Readjust R5 if necessary so that both +15 and -15 V supplies are within ±0.3 V.

Measure the +5 V supply on the RED Test Point and adjust R19 (5 V ADJ) for 5 V ±0.1 V.

Measure the -5 V supply on the GREEN Test Point and verify that it is within ±0.1 V of -5 V. Readjust R19 if necessary so that both +5 and -5 V supplies are within ±0.1 V.

4.4.3 Oscillator Adjustment

The accuracy of the oscillator may be determined, relative to a frequency standard by observing the rate of an oscilloscope pattern as shown in Figure 4.1, Oscillator Accuracy Test.

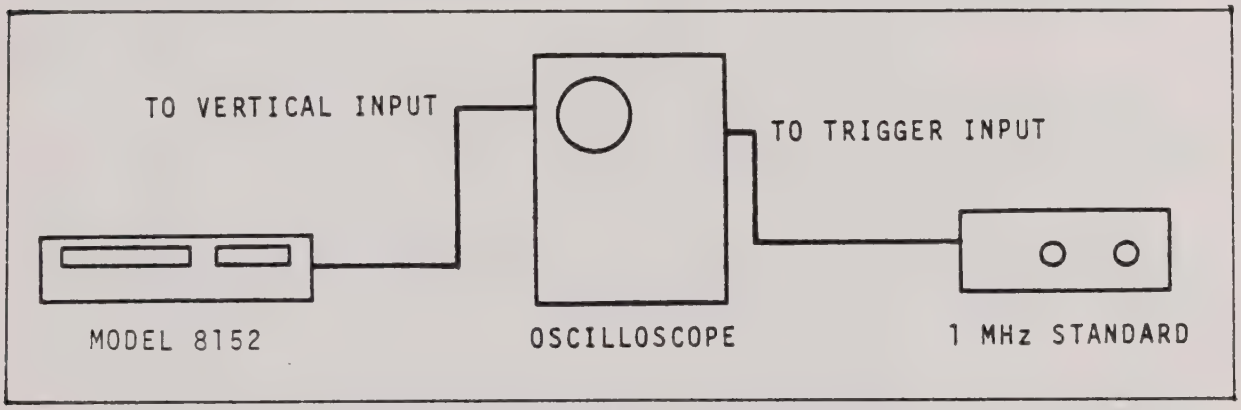


FIGURE 4.1 OSCILLATOR ACCURACY TEST

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

To check oscillator frequency (not stability):

1) Trigger the oscilloscope externally with the 1 MHz standard.

2) Connect a 1 MHz frequency from the Model 8152 to the vertical input of the oscilloscope, (pin X of Time Base and Control Card).

3) Set the oscilloscope sweep time to 0.1 µsec/cm and adjust the controls to obtain a presentation of one to two cm vertical deflection.

4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10^7. If necessary, adjust the oscillator (C3 on the Time Base and Control Card) until drift is negligible.

TABLE 4.2 OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6
1 cm/sec	1 part in 10^7
1 cm/10 sec	1 part in 10^8

4.4.4 Generate Function

1) Place the Mode selector switch in the GENerate position to ensure that the Display counts in a normal sequence.

2) Preset 23 hours, 59 minutes, 59 seconds into the Display, and note that on the next count the display becomes all 0's (if the instrument also displays days, that the days register advances to 00).

3) Repeat Step 2) and preset 009 in the Days Register and observe that on the next count the Days Register will advance to 010.

4) Repeat Step 3) to ensure correct operation for the remaining digits of the Days Register.

4.4.5 Modulator (Dwg. #021556-7-5)

1) Adjust the TUNE (R53)control for maximum ac signal at the MOD test point.

2) Adjust the MOD CODE LEVEL (R20) control for a nominal 3 V p-p, output of the Large Cycle signal.

3) Adjust the RATIO (R16) control for a 3:1 modulation ratio.

4) Return to the TUNE (R53) control and adjust until the junction point of the large and small cycles has a minimum of distortion (see Figure 4.2, Tune Control Adjustment).

5) Adjust the DC CODE LEVEL control for a nominal output of 3 V p-p at DC Test Point.

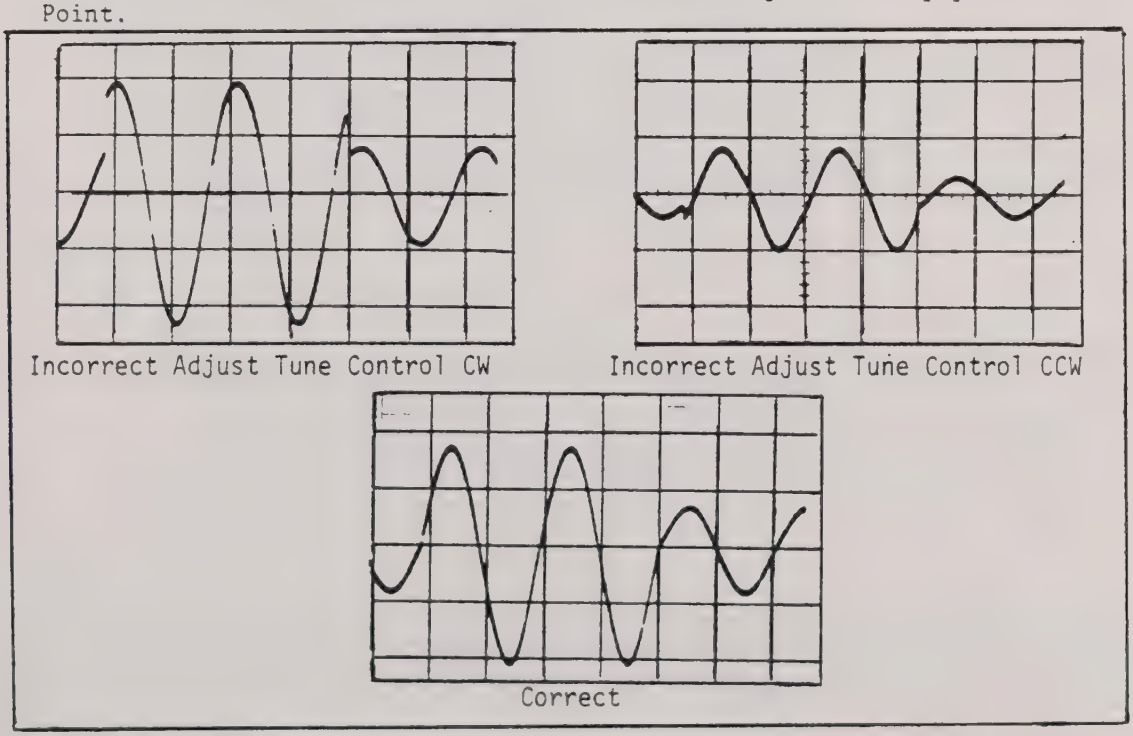


FIGURE 4.2 TUNE CONTROL ADJUSTMENT

4.4.6 AGC/Cycle Detector (Dwg. #021569-7-1)

1) Preliminary Set-Up

   a) Connect a time code source to CODE IN, BNC connector on rear panel of the unit (signal level approximately 3 V p-p).

   b) Place unit in either READ Mode.

CAUTION

Do not place AGC/Cycle Detector on extender board when performing these adjustments.

2) AGC Level

   a) Monitor "TRIG" test point with oscilloscope.

      (1) Adjust the AGC LEVEL ADJ. (R4) so that the large cycles are 2.75 V p-p ±5% (see Fig. 4.3, AGC Level Adjustment).

      (2) Reduce level of incoming time code signal to approximately 1 V p-p.

      Allow approximately 5 seconds for AGC to recover. Signal at "TRIG" test point should remain the same amplitude as adjusted in Step (1).

3) Cycle Detector

   a) Monitor "TRIG" test point with oscilloscope.

      (1) EC (Each Cycle) Adjustment

      Set oscilloscope to trigger positive (+), external trigger. Connect external trigger input of oscilloscope to EC test point.

      Turn E.C. ADJ. (R25) control full clockwise. Turn in the CCW direction until each cycle is triggering approximately 30% up on the positive slope of the small cycles (see Fig. 4.4, Cycle Detector Adjustment).

      (2) LLC (Lower Large Cycle) Adjustment

      Set oscilloscope to trigger negative (-), external trigger. Connect external trigger input of oscilloscope to $\overline{LLC}$ test point.

      Turn L.L.C. (R34) Adjust, full clockwise. Turn in the CCW direction until the lower large cycles are triggering approximately 75% of the way down on the negative slope of the lower large cycles (see Fig. 4.5, Lower Large Cycle Adjustment).

4.4.7 Reverse Operation

With the Model 8152 in either READ Mode, check that it will read in the forward and reverse directions as follows: Place the TAPE DIRECTION switch in the NORM position for a forward read direction, and in the REV position for a reverse code read direction.

4.4.8 Sensitivity

If possible, vary the input read code voltage within the limits stated in Chapter 1; observe that the unit reads the code normally in both forward and reverse directions.

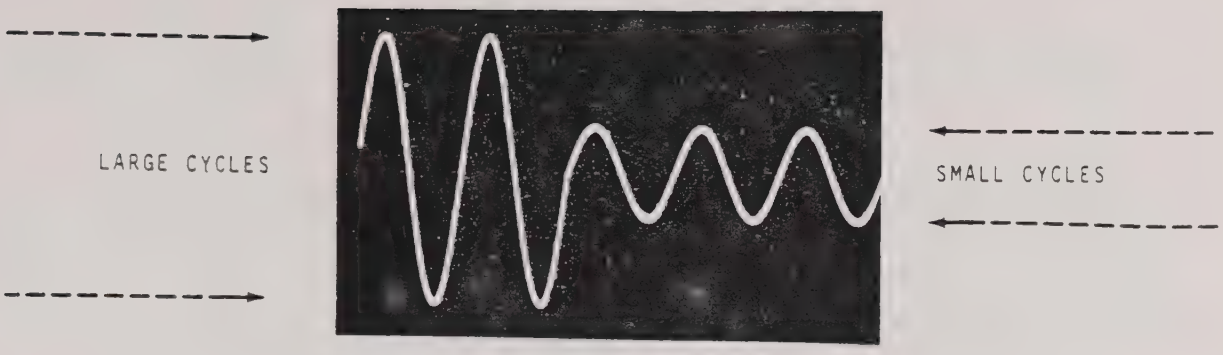


FIGURE 4.3 AGC LEVEL ADJUSTMENT

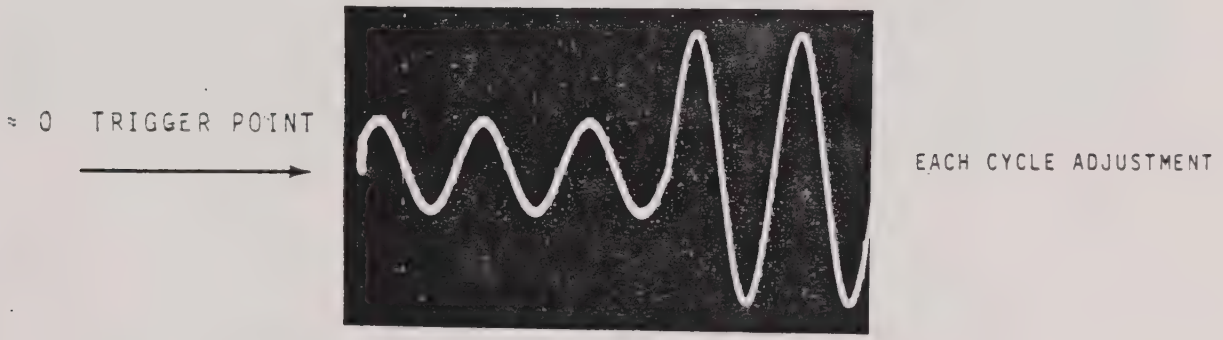


FIGURE 4.4 CYCLE DETECTOR ADJUSTMENT

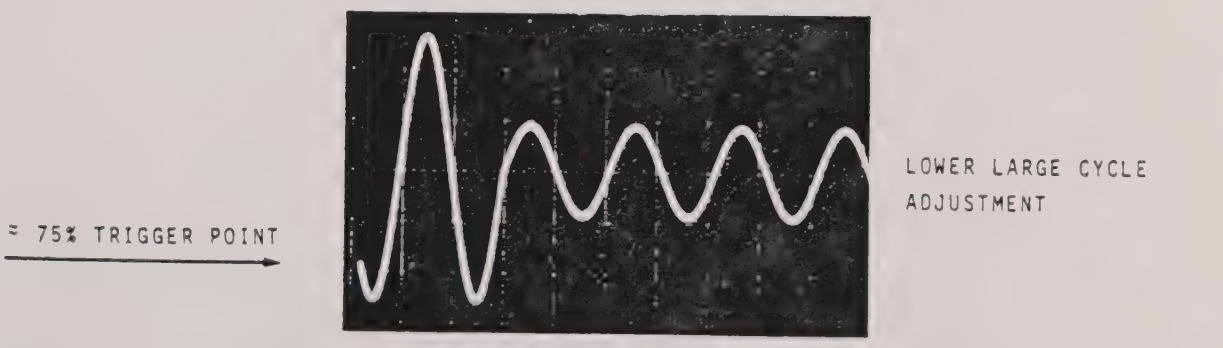


FIGURE 4.5 LOWER LARGE CYCLE ADJUSTMENT

4.4.9 Frequency Response

If possible, vary the input code voltage within the limits stated in Chapter 1; observe that the unit reads the code normally in both forward and reverse directions.

4.4.10 Error Bypass (Dwg. #7-05153802)

1) Using a separate time code generator in a HOLD mode, produce a continuous time code which is not updated. Connect this signal to the CODE IN BNC connector on the rear panel of the Model 8152.

2) Place the Model 8152 MODE selector switch in READ 3E (Error Bypass) position. Observe that the units-of-seconds updates 3 numbers and returns to the number displayed on the test unit generator.

3) Place the MODE switch in GENerate position. The translator should update in the normal manner.

4.4.11 General Checkout

No additional adjustments are required in the instrument. To facilitate tracing possible malfunctions, determine if each plug-in card is performing in accordance with the circuit description provided in other sections of this manual. It is advisable to determine proper operation of the boards in the order of decreasing signal repetition rate. Peripheral circuitry, such as thumbwheel switches, are most easily tested in conjunction with their associated plug-in boards.

CHAPTER 5
FUNCTIONAL DESCRIPTION

5.1 GENERAL

The Model 8152 is a combination Time Code Generator/Reader. These two main functions are described separately in this chapter. Schematics and specific card assembly descriptions relating to the basic unit are provided at the end of the chapter. Standard options, when included, are described in Chapter 6. Special modifications, if any, are presented in Chapter 7.

5.1.1 Reference Designations

Reference designations are confined to the assembly under discussion, since it is usually clear from the context which assembly is involved.

When citing a subsection of a multisection integrated-circuit, the reference designation of the integrated-circuit is given, followed by the number of the output terminal.

When citing flip-flops formed from two gates on the same chip, the reference designation of the chip is given followed by the two output pin numbers. The reference designations used in the instrument are listed in Table 5.1.

TABLE 5.1

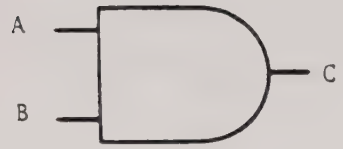
REFERENCE DESIGNATIONS

A or U	Integrated Circuit
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
FL or Z	Filter
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.1.2 Logic Functions

The Logic symbols and functions used in the Model 8150 are described as follows:

AND Gate



INVERTED NOR Gate

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND Gate and INVERTED NOR Gate have the same truth table.

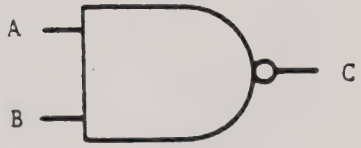
NAND Gate

INVERTED OR Gate

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The NAND Gate and INVERTED OR Gate have the same truth table.

OR Gate

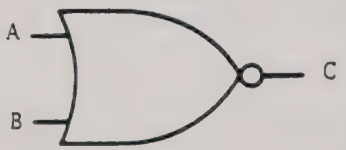


INVERTED NAND Gate

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The OR Gate and INVERTED NAND Gate have the same truth table.

NOR Gate

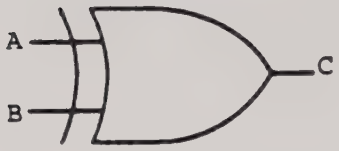


INVERTED AND Gate

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The NOR Gate and INVERTED AND Gate have the same truth table.

EXCLUSIVE OR

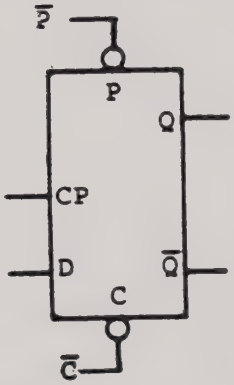


A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together.

These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line the AND or OR symbol is used only once.

DOT AND

DOT OR

5.2 GENERATOR FUNCTION

When functioning as a Time Code Generator, the Model 8152 is essentially a digital clock which generates a serial time code. A 1 MHz time base signal is divided down to 1 pps and fed to a Time-of-Day (TOD) Accumulator (Display Register) which outputs parallel, BCD time in hours, minutes and seconds. The accumulated time is displayed and provided as buffered, parallel BCD outputs at a rear panel connector. This same time information is serialized and fed to rear panel BNC connectors in DC Level Shift form and as a modified IRIG B time code on a 1 kHz carrier. (Days/ID and/or other codes may be provided as options.) Four simultaneous pulse rate outputs are also generated. Switches are provided for entering Start Time for real time operation or the unit may be operated in an elapsed time mode.

The Time Code Generator circuitry is described briefly below and in more detail in the Circuit Descriptions at the end of this chapter. The circuitry is shown, in block form, on the Block Diagram, Dwg. #7-06102806.

5.2.1 Time Base and Control (Dwg. #021566-7-9)

Referring to the Block Diagram, the Time Base and Control Card (A27) is shown at the left. This card contains the 1 MHz internal oscillator with shaper, a Start/Stop flip-flop, an Elapsed Time gate, a three-decade divider and separate TOD and Days/ID Preset/Reset circuits. The symetrical 1 kpps output (5×10^{-4}) from the Divider is fed through selection gates on the Preset and Error Bypass Card (A11), emerging as the $\overline{Z\text{-Rate}}$ signal which is fed to the Minor Counter Card (A9) and Code Generator Card (A17). The inverse of this signal is fed to the Modulator Card (A20) where it is shaped to form the 1 kHz carrier for the serial time code.

5.2.2 Minor Counter (Dwg. #021632-7-2)

The Minor Counter Card (A9) is a three-decade divider which divides the 1 kHz ($\overline{Z\text{-RATE}}$) input down to 1 pps to drive the TOD Accumulator Card (A15) and provide a sync signal for Code Generator Card (A17). Separate sets of buffers are provided for parallel BCD millisecond outputs for Option E14, Millisecond Outputs. Pulse rates (1 kpps, 100 pps, 10 pps and 1 pps) are provided at connector J4.

5.2.3 TOD Accumulator (Dwg. #021543-7-3)

The TOD Accumulator Card (A15) accepts the 1 pps (8×10^{-1}) output from the Minor Counter Card (A9) and divides it into units of tens-of-seconds, minutes and hours. The decade and scale-of-six dividers which accomplish this can be parallel preset, as well as provide parallel BCD outputs. The parallel BCD outputs feed: 1) the Display Assembly (A102; 2) the Code Generator (A17); 3) Buffer (A16) and Preset Switches S6-S11. The 1 ppd output is fed through selection gates on Modulator (A20) to Days Accumulator (A18) as part of Option E13, Days/ID. (Optional information is shown in Chapter 6.)

5.2.4 Code Generator (Dwg. #021554-7-1)

The Code Generator Card (A17) accepts the parallel TOD inputs and develops a serial level shift code complete with index and frame markers. Days/ID are replaced by zeros in the code in the absence of Option E13. The level shift code is fed to the Modulator.

5.2.5 Modulator (Dwg. #021556-7-5)

The Modulator Card (A20) modulates a synchronized 1 kHz sine wave with the serial level shift code from the Code Generator. The 1 kHz sine wave is developed by shaping the Z-RATE input previously mentioned (para. 5.2.1). The modulated and level shift (DC) codes are buffered and fed to rear panel BNC connectors. Adjustments for Mark-to-Space Ratio and Amplitude are provided.

5.3 READER FUNCTION

As a Time Code Reader, the Model 8152 accepts a serial modulated IRIG B time code input. It strips time information from the code in bytes and loads it into the TOD Accumulator. The time in the accumulator is displayed. It is also available for output in parallel BCD through buffers on Card A16. Circuits are included to maintain the accumulator on time in forward mode and to regenerate a serial code for comparison with the input in the Error Bypass mode of operation. (Days/ID and/or the translation of other time codes may be included as options.) Most of the Time Code Reader circuitry is shared with the Time Code Generator described above. It is shown on the same block diagram.

5.3.1 AGC/Cycle Detector (Dwg. #021569-7-1)

Referring to the Block Diagram, the modulated input code is fed through connector J8 to the AGC/Cycle Detector Card (A10). The AGC circuit on this card establishes a standard level signal from which two signals are derived. The first of these is the EC (Each Cycle) signal which is a square wave at the carrier frequency. The second is the $\overline{\text{LLC}}$ (Lower Large Cycle) signal. Both signals are fed to the Reader Logic Card (A12). The EC signal is also fed through selection gates on the Preset and Error Bypass Card (A11), emerging as the $\overline{\text{Z-RATE}}$ signal to the Minor Counter Card (A9) and Code Generator Card (A17).

5.3.2 Reader Logic (Dwg. #021588-7-3)

The Reader Logic Card (A12) contains a 9-bit shift register which accumulates time information stripped from the input code. This register is cleared and a ONE entered by the double-mark at the beginning of the time frame. This is followed by each subsequent bit as it is detected. When the initial ONE is in the 9 position, the contents of the shift register are transferred into the seconds section of the TOD Accumulator A15). The next index mark clears the register and enters a ONE followed by minutes information. These bits are transferred to the minutes section of the accumulator. In like manner, hours (and days) bits are detected and transferred. (Days are loaded into Days Accumulator A18.)

5.3.3 Minor Counter (Dwg. #021632-7-2)

Once the Time Code Reader is synchronized with the input code (in forward), the Accumulator, consisting of A15) plus A18 with Option E13, already contains the current information being transferred in. This is accomplished by the Minor Counter Card (A9) which derives a 1 pps, on-time update pulse from the $\overline{\text{Z-RATE}}$ signal. This signal updates the accumulator on-time at the beginning of each frame.

5.3.4 Error Bypass (Dwg. #7-05153802)

The Code Generator Card (A17) accepts the parallel TOD (and Days) information and develops a serial level shift output code as previously described for Generator Function. This code, which represents the contents of the accumulator, is compared with the incoming code in circuits on Preset and Error Bypass Card (A11) when operating in the Error Bypass mode. This circuitry inhibits the transfer of up to three consecutive input code frames when a discrepancy is detected.

5.3.5 Modulator (Dwg. #021556-7-5)

The Modulator Card (A20) supplies the regenerated DC Level Shift code as an output. When operating in real time, the regenerated modulated code is also available.

5.3.6 Reverse Code (Dwg. #021625-7-1)

The Time Code Reader is capable of reading the input code in reverse mode. The conditions for reverse read operation are established by circuits on FWD-REV Control Card (A13) in response to signals from the TAPE DIRECTION switch or the REV input through connector J3. Circuits on Card A13, invert the order in which bits are transferred to the Accumulator, suppress the 1 pps update signal and inhibit Error Bypass when reading a reverse code. In reverse, the contents of the Accumulator are no longer on-time.

5.4 CIRCUIT DESCRIPTIONS

TABLE 5.2

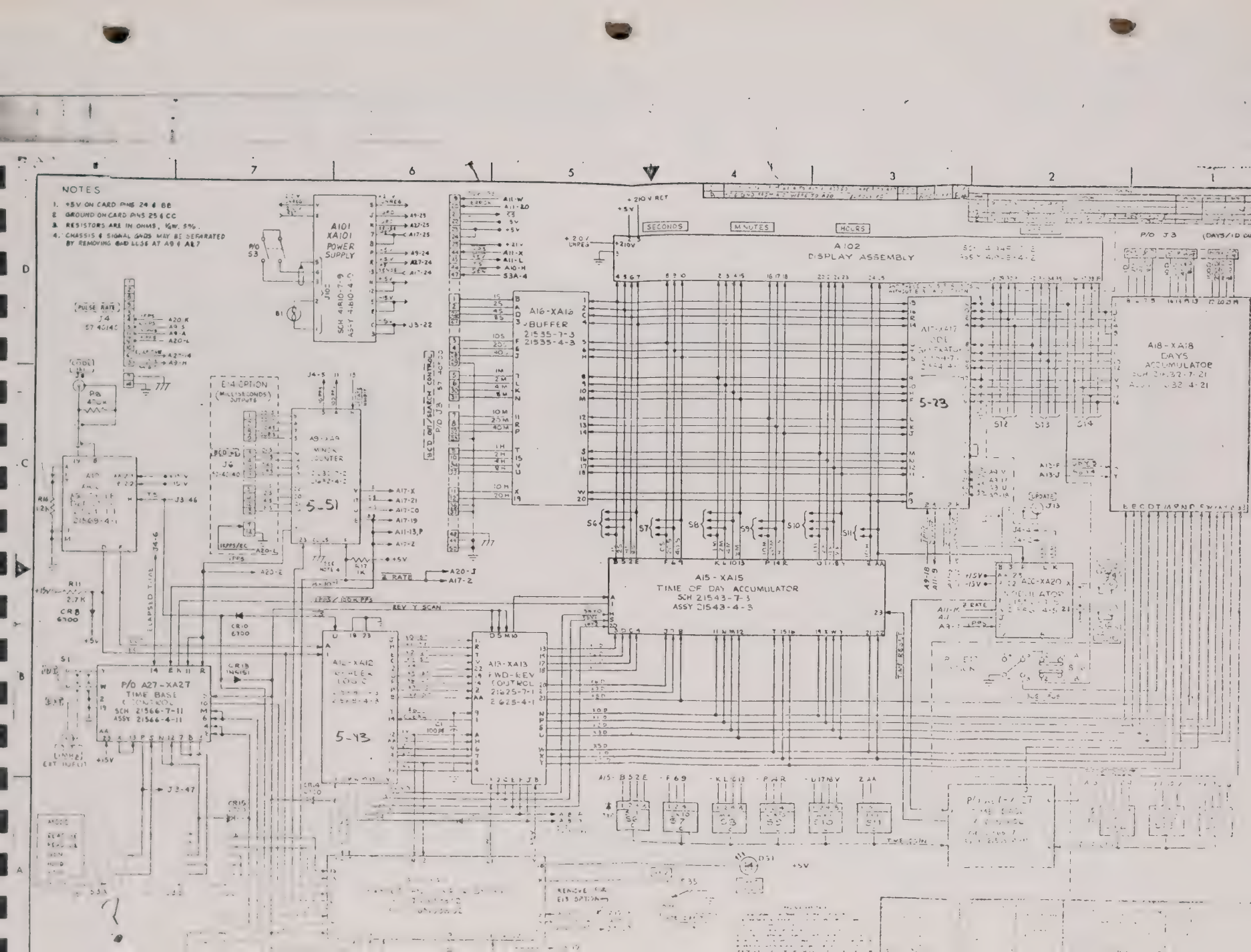
CIRCUIT DESCRIPTION INDEX INFORMATION

Location	Description	Schematic #
A1-A8	Reserved for Options	
A9	Minor Counter	021632-7-2
A10	AGC/Cycle Detector	021569-7-1
A11	Preset and Error Bypass	7-05153802
A12	Reader Logic	021588-7-3
A13	FWD-REV Control	021625-7-1
A14	Reserved for Options	
A15	TOD Accumulator	021543-7-3
A16	Buffer	021535-7-3
A17	Code Generator	021554-7-1
A18	Days Accumulator (Optional)	021632-7-21
A19	Reserved for Options	
A20	Modulator	021556-7-5
A21-A26	Reserved for Options	
A27	Time Base and Control	021566-7-11
A101	Power Supply	041810-7-9
A102	Display Assembly	041945-7-2

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to ensure that a card is installed in the correct card slot. Extractor handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board, it is possible to install the card backwards which will result in serious damage.


NOTES
1. +5V ON CARD PINS 24 & BB
2. GROUND ON CARD PINS 25 & CC
3. RESISTORS ARE IN OHMS, ¼W, 5%.
4. CHASSIS & SIGNAL GNDS MAY BE SEPARATED BY REMOVING GND LUG AT A9 & A27
A101 XA101 POWER SUPPLY
SCH 4A10-7-9
ASSY 4A10-4-9
A102 DISPLAY ASSEMBLY
SECONDS
MINUTES
HOURS
A16-XA16 BUFFER
21535-7-3
21535-4-3
A18-XA18 DAYS ACCUMULATOR
A15-XA15 TIME OF DAY ACCUMULATOR
SCH 21543-7-3
ASSY 21543-4-3
A14-XA14 MINUTE COUNTER
A13-XA13 FWD-REV CONTROL
21625-7-1
21625-4-1
A12-XA12 DECADE LOGIC
P/O A27-XA27 TIME BASE CONTROL
SCH 21566-7-11
ASSY 21566-4-11
A9-XA9 HOUR COUNTER
A17-XA17 MINUTE DECODE
A11-XA11 SECONDS DECODE
A10-XA10 HOURS DECODE
A8-XA8 DISPLAY DRIVER
A7-XA7 DISPLAY DRIVER
A6-XA6 DISPLAY DRIVER
A5-XA5 DISPLAY DRIVER
A4-XA4 DISPLAY DRIVER
A3-XA3 DISPLAY DRIVER
A2-XA2 DISPLAY DRIVER
A1-XA1 DISPLAY DRIVER
A20-XA20 ACCUMULATOR
A19-XA19 ACCUMULATOR
A21-XA21 ACCUMULATOR
A22-XA22 ACCUMULATOR
A23-XA23 ACCUMULATOR
A24-XA24 ACCUMULATOR
A25-XA25 ACCUMULATOR
A26-XA26 ACCUMULATOR
P/O A27-XA27 TIME BASE CONTROL
SCH 21566-7-11
ASSY 21566-4-11

PARTS LIST

FINAL ASSEMBLY #06102806

REF.	DESCRIPTION	SD PART NO.
	Assembly, Shipping	06102806
	Assembly, Test	6113404
	Cover, Top	03376005
	Cover, Bottom	03376105
	Window	051001-1-1
	Cover, Mounting Bracket	039857
	Trim, Front Panel	041997-1-1
	Trim, End Rack Mount	03995202
	Trim, End Rack Mount	03995202
	Handle	100927
P3	Connector, 50-pin	101157
P4	Connector, 14-pin	101181
	Cord, Line	102407
	Assembly, Test	06113404
	Assembly, Front Panel	06113604
	Assembly, Rear Panel	06113501
A1	Extender	021507-4-1
A9	Assembly, Minor Counter	021632-4-2
A10	Assembly, AGC/Cycle Detector	021569-4-1
A11	Assembly, Preset & Error Bypass	05153802
A12	Assembly, Reader Logic	021588-4-3
A13	Assembly, FWD/REV Control	021625-4-1
A14	Not Used	
A15	Assembly, TOD Accumulator	021543-4-3
A16	Assembly, Buffer	021535-4-3
A17	Assembly, Code Generator	021554-4-1
A18	Not Used	
A19	Not Used	
A20	Assembly, Modulator	021556-4-5
A21-26	Not Used	
A27	Assembly, Time Base	021566-4-11
A101	Assembly, Power Supply	041810-4-9
C1	Capacitor, 100 pF DM	100173
CR8,10,12,14-16	Diode, 6700	006700
CR13	Diode, 1N4151	100385
R8	Resistor, 470 k 5%, 1/4 W, CC	101630
R11	Resistor, 2.7 k 5%, 1/4 W, CC	101599
R16	Resistor, 1.2 k 5%, 1/4 W, CC	101581
R17-18	Resistor, 1 k 5%, 1/4 W, CC	101569

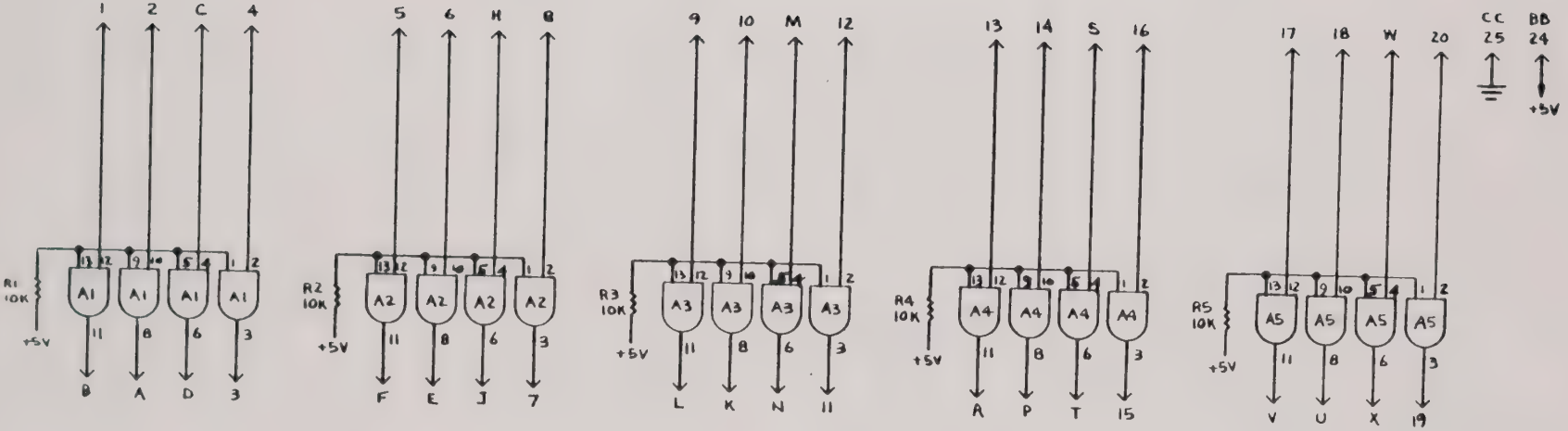
PARTS LIST
FINAL ASSEMBLY #06102806 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
	Assembly, Test (Cont'd)	06113401
XA1,9-17,20,27	Connector, PC Edge	101204
XA101	Connector, 22-pin Dual	101167
	Connector, 5-pin Molex	101263
	Connector, Male Pin	10282202
	Card Rack, Front	051005-1-1
	Card Rack, Rear	051005-1-2
	Gusset, Left	041809-1-1
	Gusset, Right	041809-1-2
	Spacer, Power Supply	051121-1-1
	Assembly, Front Panel	06113604
	Assembly, Display	041945-4-2
	Sub Front Panel	061171
DS1	Lamp, LED	100456
S3	Switch, Rotary	06134402
S4	Switch, Toggle	102333
S6,8,10	Switch, Thumbwheel	05130011
S7,9,11	Switch, Thumbwheel w/colon	0513002
S12-14	Switch, Spacer	102358
S35	Switch, Toggle SPDT	102310
	Switch, End Bracket	102359
	Switch, Strap	10236709
	Knob	102954
	Dress Nut	100893
	Assembly, Rear Panel	06113501
	Panel, Rear	041815-1-2
B1	Fan, 50-60 Hz	100038
J3	Connector, 50-pin	101156
J4	Connector, 14-pin	101180
J8-12	Connector, BNC	101155
S1	Switch, Slide	102630
S15	Switch, Cover Plate	05120801
S16	Switch, Cover Plate	05120802
	Plate, Cover Oscillator	051913
	Fan, Screen	100886
	Plug, BNC Hole	100952
	Cover Plate, 14-pin	021398-1-1
	Cover Plate, 36-pin	031124-1-1
	Cover Plate, 50-pin	031394-1-1
	Insulator, BNC	100823
	Washer, Fiber	101074
	Eyelet (for S1)	112482
	#6 Flat Washer	100704

CIRCUIT DESCRIPTION
BUFFER
SCHEMATIC #021535-7-3

1) GENERAL

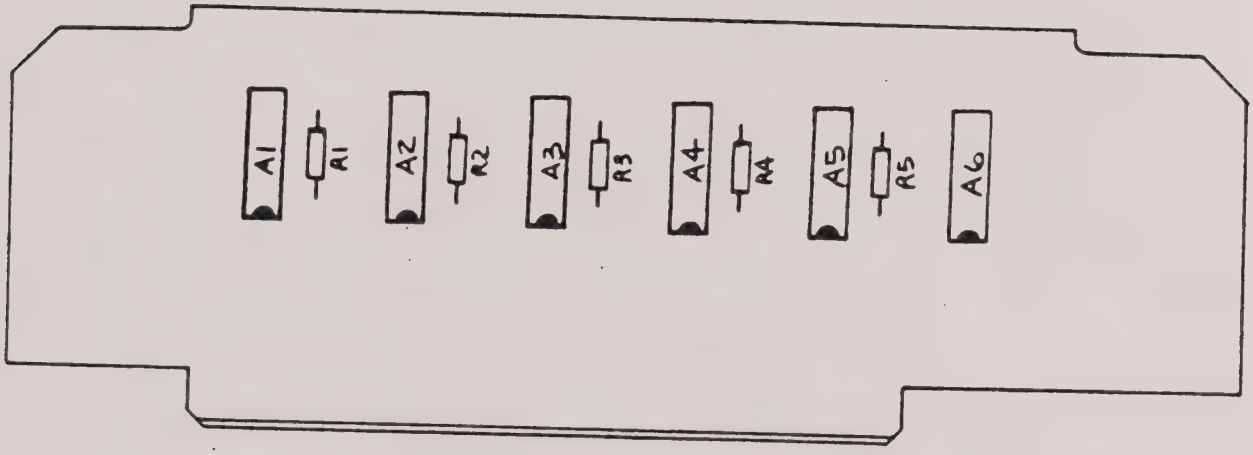
This card contains twenty integrated circuit gates, connected as noninverting buffers. It is used to buffer hte seconds through hours outputs of the Time-of-Day accumulators. A binary "1" output is 5 V (±0.5 V) 6 kΩ source. A binary "0" output is 0 V (±0.5 V, 15 mA sink).



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GRD.
3. A1 THRU A5 ARE MC1806P.

BUFFER SCHEMATIC #021535-7-3 REV A



BUFFER ASSEMBLY #021535-4-3 REV 1

PARTS LIST

BUFFER #021535-7-3

REF.	DESCRIPTION	SD PART NO.
	Assembly	021535-4-3
	Schematic	021535-7-3
A1-5	Integrated Circuit, MC1806P	025733
R1-5	Resistor, 10 k 5%, 1/4 W	101570
	Extractor	100865

CIRCUIT DESCRIPTION
TIME-OF-DAY ACCUMULATOR
SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, and input inhibit circuit is provided, and the hours dividers are recycled at 23:59:59.

2) DIVIDERS

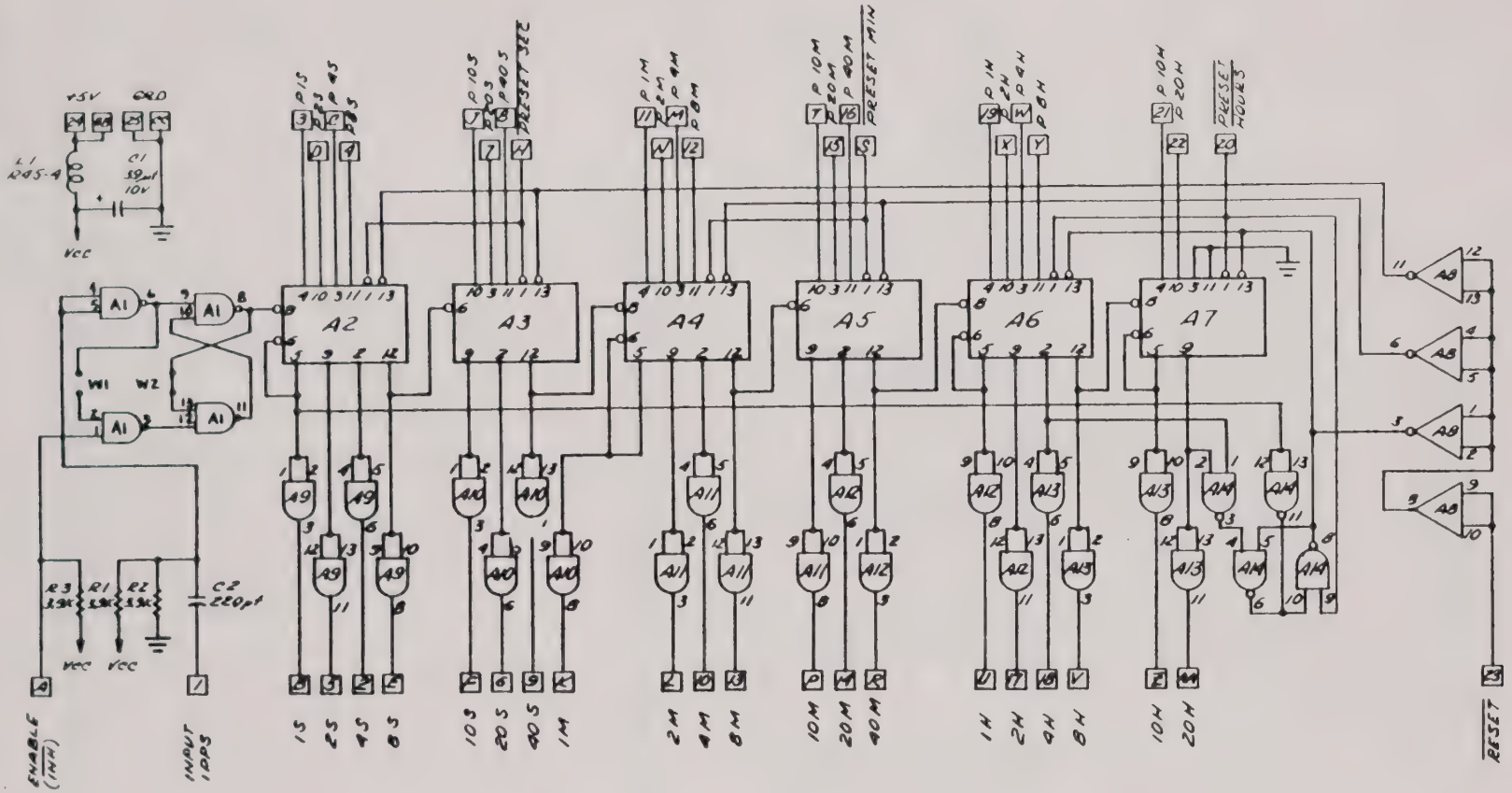
Dividers A2, A4, A6 and A7 are divide-by-10 circuits. Dividers A3 and A5 are divide-by-6 circuits. Each divider has its data inputs connected to a preset time source. Grounding the appropriate preset line will load the preset time into the divider. Inverters A8 are used to buffer the seconds reset lines.

3) INHIBIT CIRCUIT

The Inhibit Circuit is used to stop updating of the accumulator when the front panel MODE Switch is in the HOLD position, if present. Gate A1-6 inverts the 1pps input. Gates A1-11/A1-8 form an RS flip-flop. Gate A1-3 inverts the $\overline{\text{INHIBIT}}$ line. When the accumulator is updating, A1-11/A1-8 output follows the 1 pps input. When the INHIBIT/ENABLE line, pin A, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE line

4) RECYCLE CIRCUIT

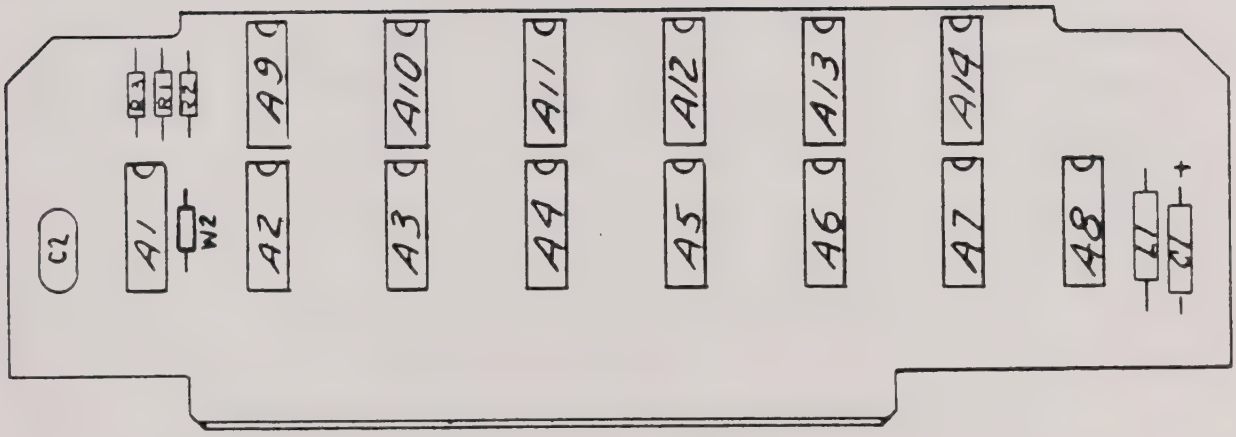
Gates A14-6/A14-8 are connected as an RS flip-flop to control the reset lines of dividers A6 and A7 for a recycle at 23:59:59. Gate A14-3 NANDS the 20-hour and the 4-hour outputs to provide a low output at 24-hours. The flip-flop (A14-6/A14-8) output will also go low, resetting A6 and A7 at this time, provided the $\overline{\text{PRESET HOURS}}$ line is high. In this way, recycle is inhibited during preset. Gate A14-11 is wire AND-connected to the flip-flop and maintains the reset pulse for one second. This allows all the flip-flops in the dividers time to reset. Reset may also be initiated from the $\overline{\text{RESET}}$ line via A8-3



NOTES:

1.) PIN 7 IS CONNECTED TO GRD ON ALL I.C.'S.
2.) PIN 14 " " " VCC " " "
3.) A2, A4, A6, A7 ARE N8280A
A3, A5 ARE C2125-A
A1, A8, A14 ARE MC896P
A10, A11, A12, A13, A9 ARE MC1806P

TIME-OF-DAY ACCUMULATOR SCHEMATIC #021543-7-3 REV B



TIME-OF-DAY ACCUMULATOR ASSEMBLY #021543-4-3 REV A

PARTS LIST

TIME-OF-DAY ACCUMULATOR #021543-7-3

REF.	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
A1,8,14	Integrated Circuit, MC846P	019716
A2,4,6,7	Integrated Circuit, N8280A	025722
A3,5	Integrated Circuit, N8288A	025723
A9-13	Integrated Circuit, MC1806P	025733
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF	100220
L1	Inductor, R45-4	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W, CC	101601
W2	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #021554-7-1

1) GENERAL

The IRIG DC Code Generator Card can be used to generate the IRIG A,B,C,E or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card.

2) DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divider-by-2, then-by-5 counter which divides down the "Z" RATE and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-5, then-by-2 counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-2, then-by-6 counter. Its principle function is to control the secondary scan gate A4. The divide-by-12 is used only for IRIG C, the divider being reset at the count of 10 or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet 2 is simply eliminated when the divider resets at 10. Reset at 10 is established by gate A18-8. A one-shot (A18012,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-5 counter provided for external use. It is synchronized with the other divider chips.

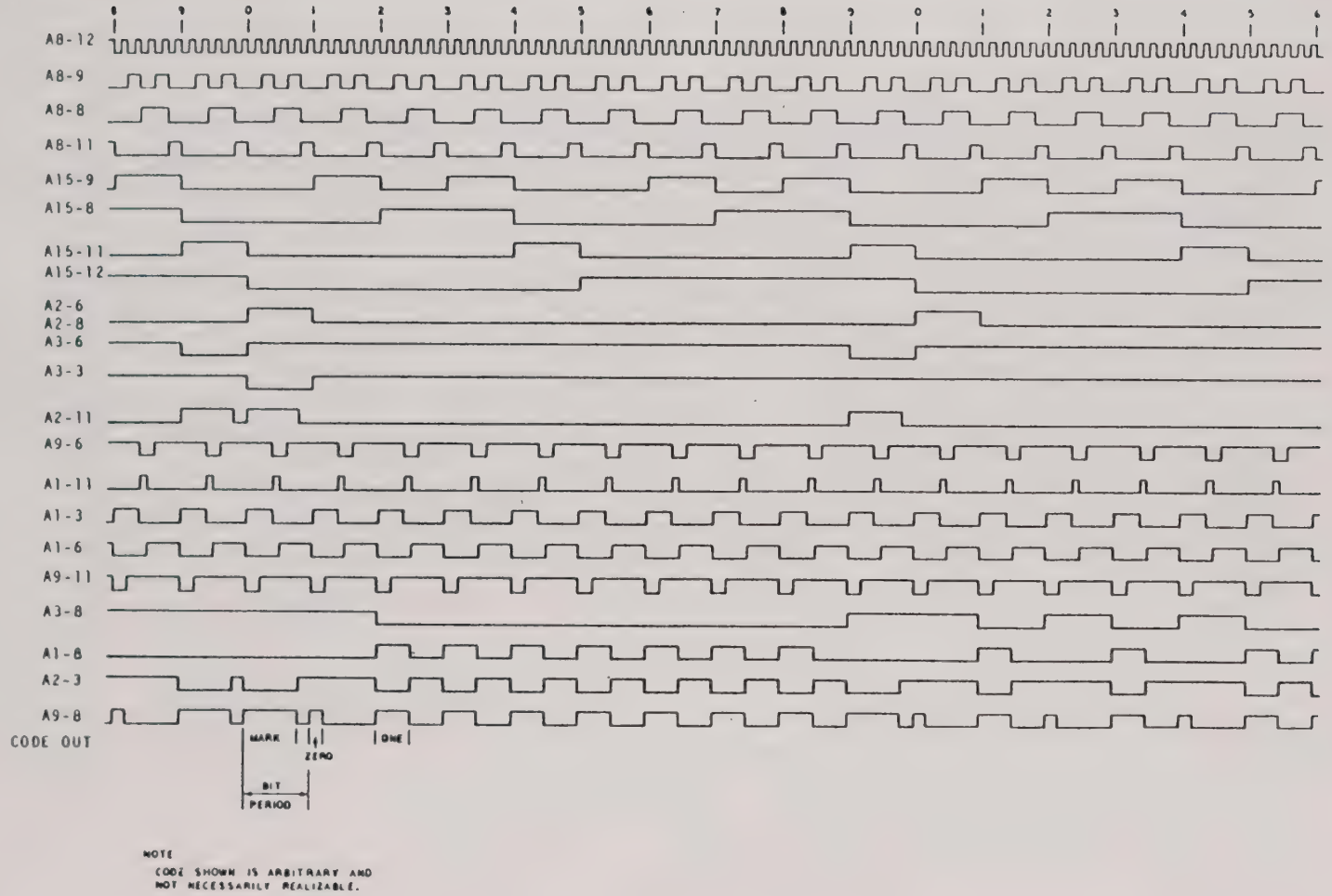
3) SCAN GATES

Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position swtiches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for switch A4. This switch, controlled from BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11 and A3-8 are used to inhibit the presence of serials ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

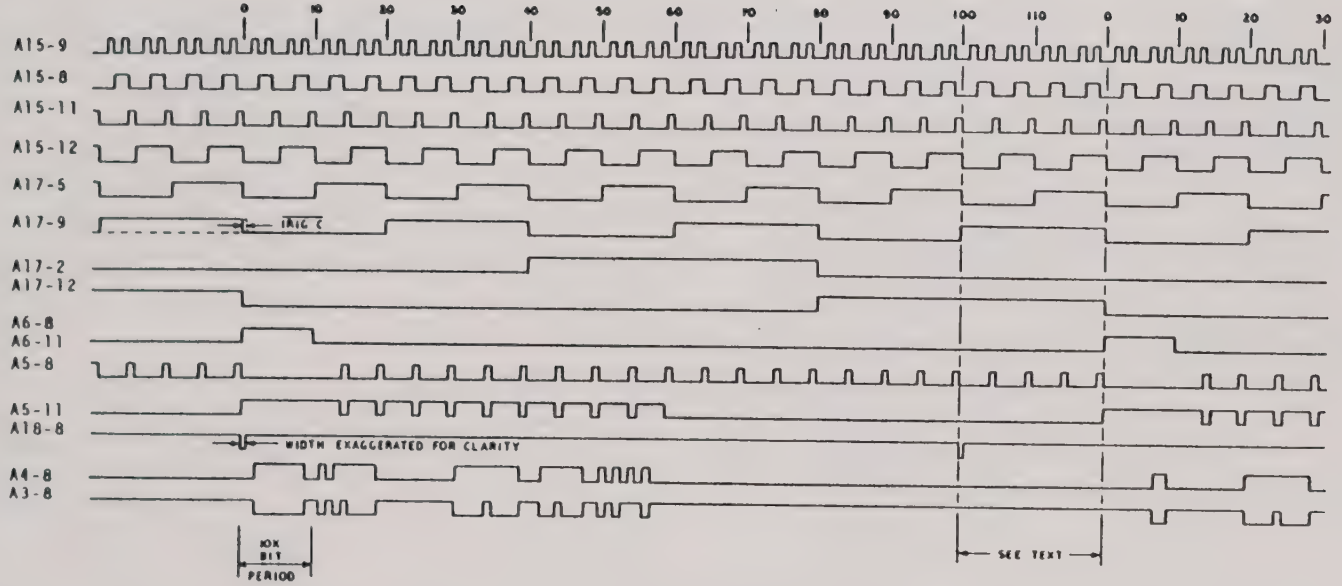
4) CODE GENERATING GATES

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE and an "8" is an INDEX MARKER.

The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. If a Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the SERIAL ONES from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.

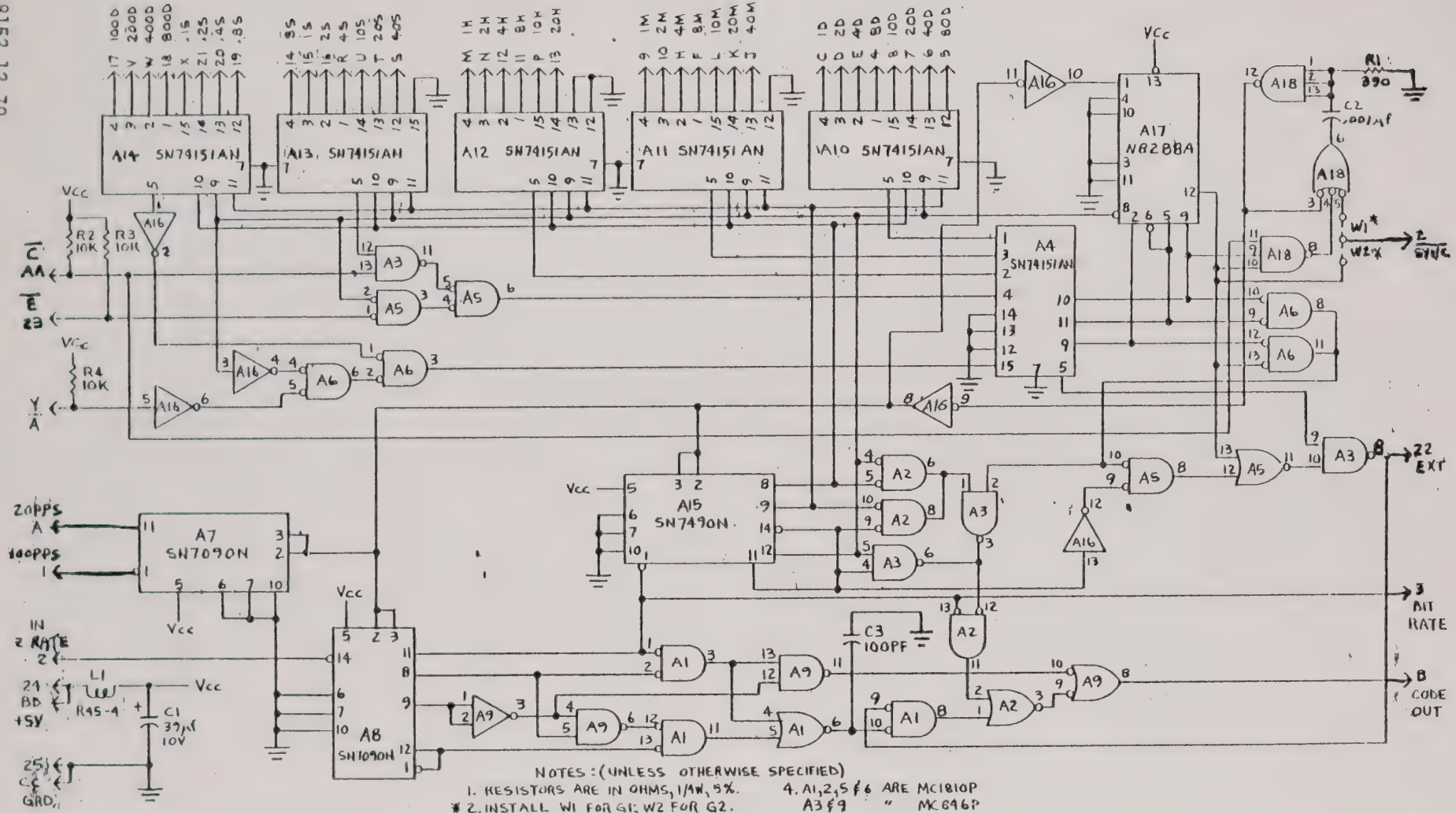


TIMING DIAGRAM - IRIG DC CODE GENERATOR (Sheet 1 of 2)

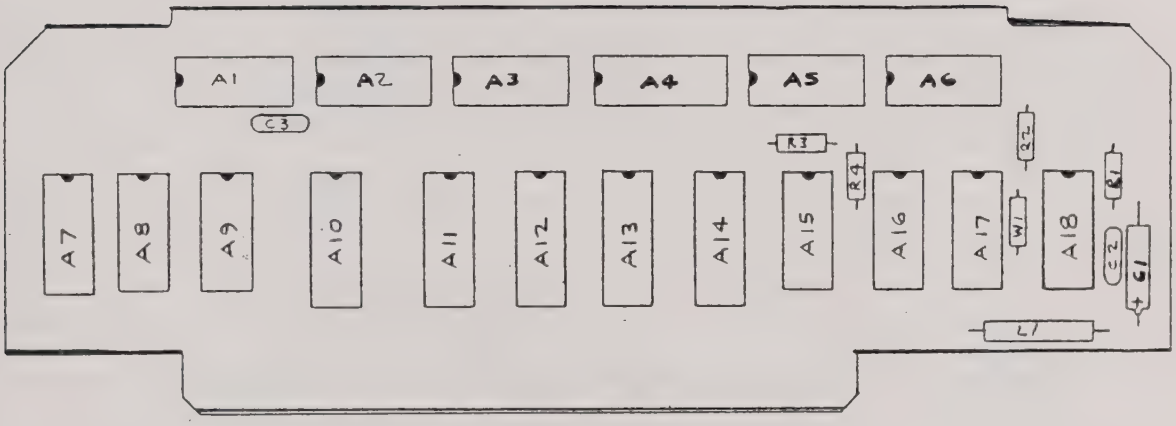


NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

TIMING DIAGRAM - IRIG DC CODE GENERATOR (Sheet 2 of 2)



CODE GENERATOR SCHEMATIC #021554-7-1 REV E



CODE GENERATOR ASSEMBLY #021554-4-1 REV D

PARTS LIST

CODE GENERATOR #021554-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1	Integrated Circuit, MC1810P	025735
A2	Same as A1	
A3	Integrated Circuit, MC846P	019716
A4	Integrated Circuit, SN74151AN	02577101
A5	Same as A1	
A6	Same as A1	
A7	Integrated Circuit, SN7490N	025732
A8	Same as A1	
A9	Same as A3	
A10	Same as A4	
A11	Same as A4	
A12	Same as A4	
A13	Same as A4	
A14	Same as A4	
A15	Same as A7	
A16	Integrated Circuit, N8288A	025723
A17	Integrated Circuit, N8288A	025723
A18	Integrated Circuit, SN7410N	019706
C1	Capacitor, 39 µF, 10 V, Tant	100183
C2	Capacitor, .001 µF Disc	100076
C3	Capacitor, 100 pF, DM15	100173
L1	Inductor, R45-4	
R1	Resistor, 390 Ω 5%, 1/4 W	101592
R2	Resistor, 10 k 5%, 1/4 W	101570
R3	Same as R2	
R4	Same as R2	
W1	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
MODULATOR
SCHEMATIC #021556-7-5

1) GENERAL

The Shaper & Modulator CArd can be assembled to provide up to 3 shaper circuits, a modulator, a dc code output buffer, a Days/ID control circuit, a square-wave decoder and miscellaneous inverters and buffers. The shaper circuits are identical with the exception that 3 capacitors within each circuit are a function of frequency. The specific assembly used is covered by the attached schematic assembly and parts list.

2) SHAPERS

Each of the shaper circuits (up to 3) are identical, with the exception that the values chosen for 3 capacitors in each circuit are inversely proportional to the resonant frequency. Each shaper accepts a logic level square-wave at the selected carrier frequency and outputs an in-phase sinewave which may be selected (through switching external to the card) and fed to the modulator. The input is filtered and applied to the base of a constant-current amplifier which drives an active circuit having the electrical properties of a tuned tank circuit. A potentiometer is provided to adjust the resonant frequency. The sinewave output from this circuit is buffered and ac-coupled to the output pin M, S or T.

3) MODULATOR

The modulator accepts the selected carrier sinewave at pin W and modulates it with the dc level shift code at pin F. The resulting modulated code is fed through amplifier A4 to output pin X.

A MODULATION RATIO adjustment, R16, sets the percentage of modulation before the signal is fed to A4. A MODULATED CODE AMPLITUDE adjustment, R20, determines the gain of amplifier A4, thus, establishing the signal level at pin X. (0 to 10 V p-p.)

4) DC CODE BUFFER

The dc level shift code input to pin F is inverted once by A1-11 and again by Q4 before being fed as the dc code output to pin 21, through R25. Transistors Q2 and Q3 and the DC CODE AMPLITUDE potentiometer R23 establish the output level at pin 21 (0.4 V to +10 V). Short-circuit protection is provided by CR3, CR4 and R24. The quiescent current in Q3 and Q4 is determined by CR3, CR5 and R25.

5) DAYS/ID (RUN NUMBER) CONTROL

Gates on A3 control the selection of the signal which is used to update the days accumulator in the system. The carry output from the TOD Accumulator is inverted and applied to A3-9. If the other input (the $\overline{\text{IN NUM}}$ line) is high (i.e., left open), the hours accumulator carry signal will update the days accumulator. Similarly, a high on the DYAS line permits a signal on pin B (ID NUM ADV) to update the days accumulator. The ID advance input pulses are standardized by one-shot A3-3, 6 to ensure reliable operation.

6) BUFFERS

Extra gates on A1 are made available for external use as inverters and buffers.

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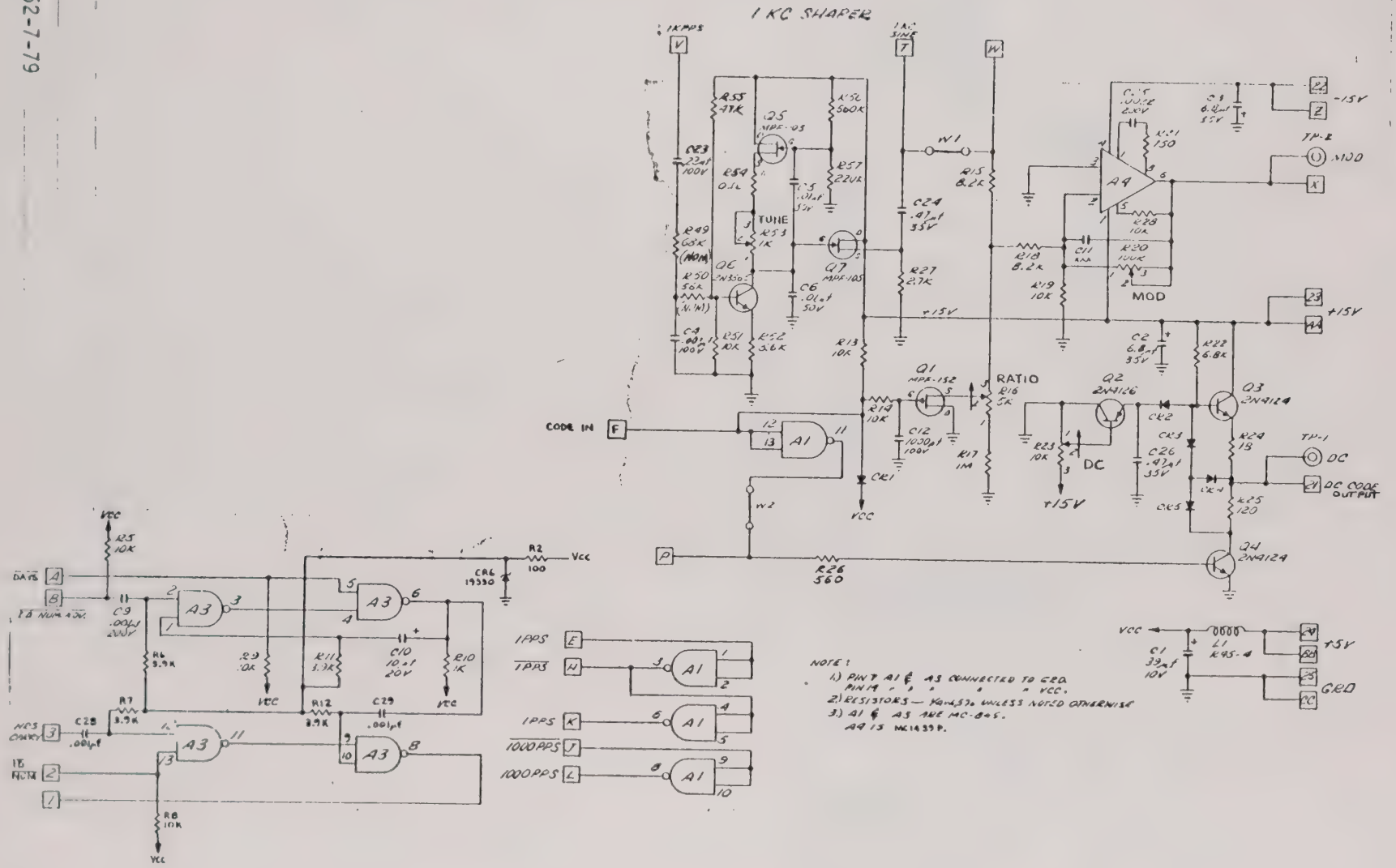
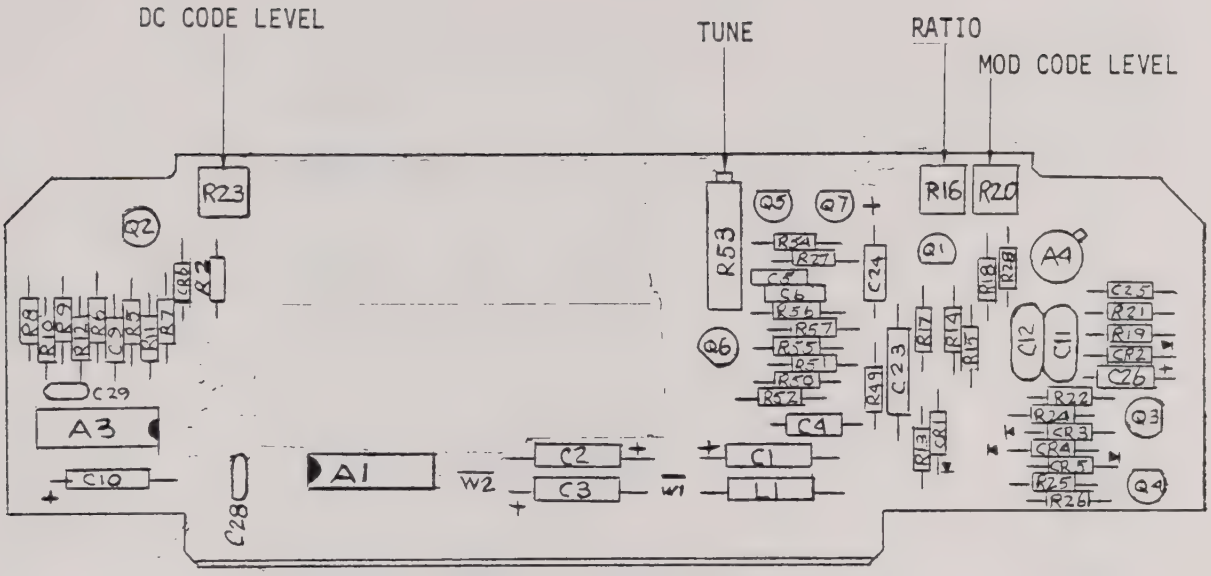


MODULATOR SCHEMATIC #021556-7-5 REV D

5-27



MODULATOR ASSEMBLY #021556-4-5 REV D_1

PARTS LIST

MODULATOR #021556-7-5

REF.	DESCRIPTION	SD PART NO.
	Assembly	021556-4-5
	Schematic	021556-7-5
A1-3	Capacitor, 39 µF, 10 V	019710
A4	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 6.8 µF, 35 V	100182
C4	Capacitor, .0033 µF, 100 V	100153
C5,6	Capacitor, .01 µF, 50 V	100132
C9	Capacitor, .001 µF, 200 V	100137
C10	Capacitor, 10 µF, 20 V	100063
C11	Capacitor, Factory Selected	CXXXXX
C12	Capacitor, 1000 pF, 100 V	100243
C23	Capacitor, .22 µF, 100 V	100148
C24,26	Capacitor, .47 µF, 35 V	100140
C25	Capacitor, .0022 µF, 200 V	100185
C28	Capacitor, .001 µF, Disc	100076
C29	Capacitor, .01 µF, Disc	100103
CR1-5	Diode, 1N4151	100385
CR6	Cioce, 193300	019330
L1	Inductor, R45-4	101313
Q1	Transistor, MPF-152	101383
Q2	Transistor, 2N3906	101378
Q3,4	Transistor, 2N3904	101377
Q5,7	Transistor, MPF-105	101384
Q6	Transistor, 2N3565	101371
R2	Resistor, 100 Ω 5%, 1/4 W, CC	101609
R5,8,9,13,14,19, 28,51	Resistor, 10 k 5%, 1/4 W, CC	101570
R6,7,11,12	Resistor, 3.9 k 5%, 1/4 W, CC	101601
R10	Resistor, 1 k 5%, 1/4 W, CC	101569
R15,18	Resistor, 8.2 k 5%, 1/4 W, CC	101595
R16	Potentiometer, 5 k, 62 PA	101845
R17	Resistor, 1 M 5%, 1/4 W, CC	101605
R20	Potentiometer, 100 k, 62 PA	101934
R21	Resistor, 750 Ω 5%, 1/4 W, CC	101689
R22	Resistor, 6.8 k 5%, 1/4 W, CC	101544
R23	Potentiometer, 10 k, 62 PA	101937
R24	Resistor, 18 Ω, 1/4 W, CC	101727
R25	Resistor, 120 Ω 5%, 1/4 W,CC	101717
R26	Resistor, 560 Ω 5%, 1/4 W, CC	101583
R27	Resistor, 2.7 k 5%, 1/4 W, CC	101599

PARTS LIST

MODULATOR #021556-7-5 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R49	Resistor, 68 k 5%, 1/4 W, CC	101597
R50	Resistor, 56 k 5%, 1/4 W, CC	101670
R52	Resistor, 5.6 k 5%, 1/4 W, CC	101584
R53	Potentiometer, 1 k 79 P	102181
R54,W1,2	Wire, Insulated #24	
R55	Resistor, 47 k 5%, 1/4 W, CC	101574
R56	Resistor, 560 k 5%, 1/4 W, CC	101687
R57	Resistor, 220 k 5%, 1/4 W, CC	101610
	Extractor	100865

CIRCUIT DESCRIPTION
TIME BASE/SERIAL PRESET-RESET
SCHEMATIC #021566-7-11

1) General

The Time Base/Serial Preset-Reset Card contains the time base circuitry and two identical circuits for independent preset of the TOD and Days Accumulators.

2) TIME BASE

The Time Base section consists of an unheated crystal, Y1, and feedback amplifier A1. The oscillator output, at pin Y, may be utilized as an external reference or it may be jumpered to pin W for internal use on the card. An external reference signal may be utilized by applying it to pin W in place of the above signal.

The time base signal is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, then fed to the base of Q3. Clipper-circuit Q3 provides a 5 V p-p square wave at pin X.

3) DIVIDER CHAIN

Control gate A5-6 receives the output of Q3 or the external reference via pin 13 depending upon which is selected.

The time base pulse rate at this point is 1 Mpps. Control gate A5-6 has two other inputs. One is the Elapsed Time input from pin 14 and the other is from Stop/Start flip-flop A4-5.

When a logic 0 (ground) is applied to the External Stop line (pin T), flip-flop A4-3 will generate a Logic 0 which will close gate A5-6 and inhibit the time base input to the divider chain. A positive transition on pin 11 or R, (the Stop time input) will also inhibit the time base if pin S is at ground.

A ground signal on the $\overline{\text{START}}$ pin 12 will set A4-5 and open gate A5-6.

The divider chain consists of three divider chips (A12, A13 and A6) connected in tandem. They divide the 1 Mpps time base down to 1 kpps. The first two (A12 and A13) are connected as divide-by-5, then-by-2 counters. These develop 100 kpps and 10 kpps square waves at pins 20 and 15, respectively. The third decade (A6) is connected in the normal divide-by-2, then-by-5 arrangement. BCD outputs (1-2-4-8) are provided at pins 21, U, V and 17. Flip-flop A4-9 develops complementary 1 kpps square wave outputs at pins 10 and 9.

Pin 2 is the zero reset input to A12. The zero reset inputs to A13 and A6 are connected to pin 19. These lines must be grounded if not in use.

4) PRESET OPERATION

Operations of the Time-of-Day Preset and Days Preset circuits are identical and only the Time-of-Day circuit will be described.

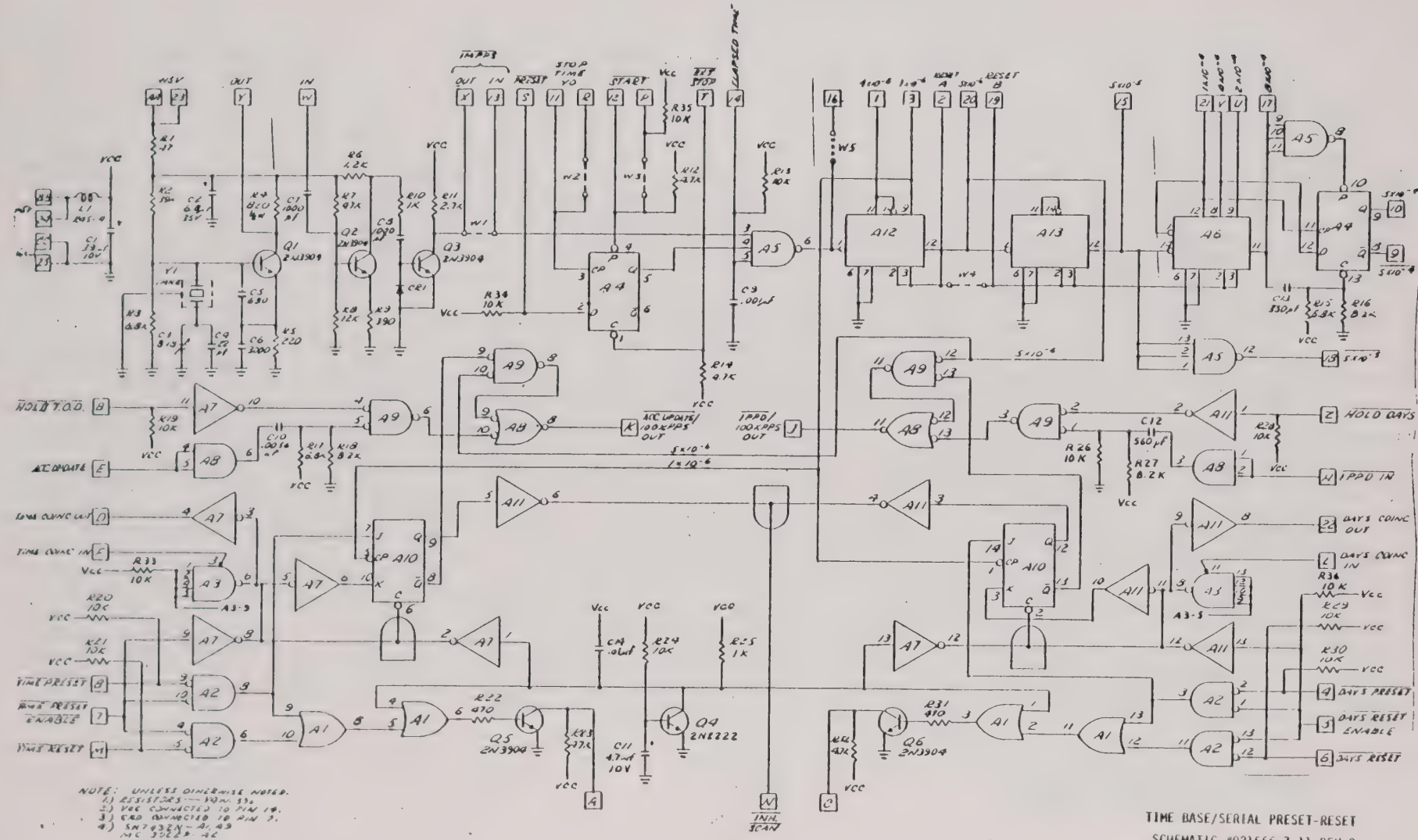
During normal operation of the Generator, the preset circuits connect the normal update inputs to their respective accumulators. In the case of the TOD Preset circuit this is the $\overline{1}$ pps input to pin E which is buffered by A8-6 then differentiated and fed to the TOD Accumulator through A9-6, A8-8 and pin K. (See Schematic.)

To initiate a TOD Preset cycle the $\overline{\text{Enable}}$ input to pin 7 must be at ground. (This condition exists in the STOP or HOLD positions of the MODE switch.) A ground on pin 7 opens gates A2-6 and A2-8 and removes the clear input to flip-flop A10-9 through inverter A7-8. The actual preset cycle is started when the PRESET/RESET switch is moemntarily thrown to the PRESET position grounding pin 8. The 2-8 output goes positive enabling the J input to flip-flop A10-9 and resetting the TOD Accumulator through A1-9, A1-6, Q5 and pin A. The next negative transition of the 500 kpps (1×10^{-6}) clock input sets flip-flop A10-9 and opens gate A9-8 to the 100 kpps (5×10^{-6}) pulse train feeding these signals to the TOD Accumulator update input through A8-8 and pin K.

The accumulator begins to update as soon as the PRESET/RESET switch is opened removing the rest. The parallel BCD outputs from the TOD Accumulator are compared in the preset thumbwheel switches with the preset start time. The switch commons are connected together and fed to pin F as the time coincidence input. This line goes positive upon detecting coincidence. The A3-6 output goes to ground driving the K input to flip-flop A10-9 positive through inverter A7-6. Flip-flop A10-9 is cleared on the next negative transition of the 500 kpps clock closing gate A9-8. The TOD Accumulator is now set to the preset start time.

4) RESET OPERATION

The accumulator is reset to zero when power is first turned on in the system. This occurs in the interval before capacitor C11 charges turning on Q4. The TOD Accumulator may also be reset when pin 7 is at ground by momentarily grounding pin M.



NOTE: UNLESS OTHERWISE NOTED.
1) RESISTORS — 1/4W, 5%
2) VCC CONNECTED TO PIN 14.
3) GND CONNECTED TO PIN 7.
4) SN7438N — A1, A3
SN7400N — A2
SN7404N — A3
SN7410N — A5
SN7420N — A6
SN7430N — A7
SN7440N — A8
SN7408N — A9, A12, A13 (VCC TO PIN 14, GND TO PIN 7)
SN7490N — A10, A11
SN7493N — A4
VCC TO PIN 5, GND TO PIN 10)

TIME BASE/SERIAL PRESET-RESET
SCHEMATIC #021566-7-11 REV B

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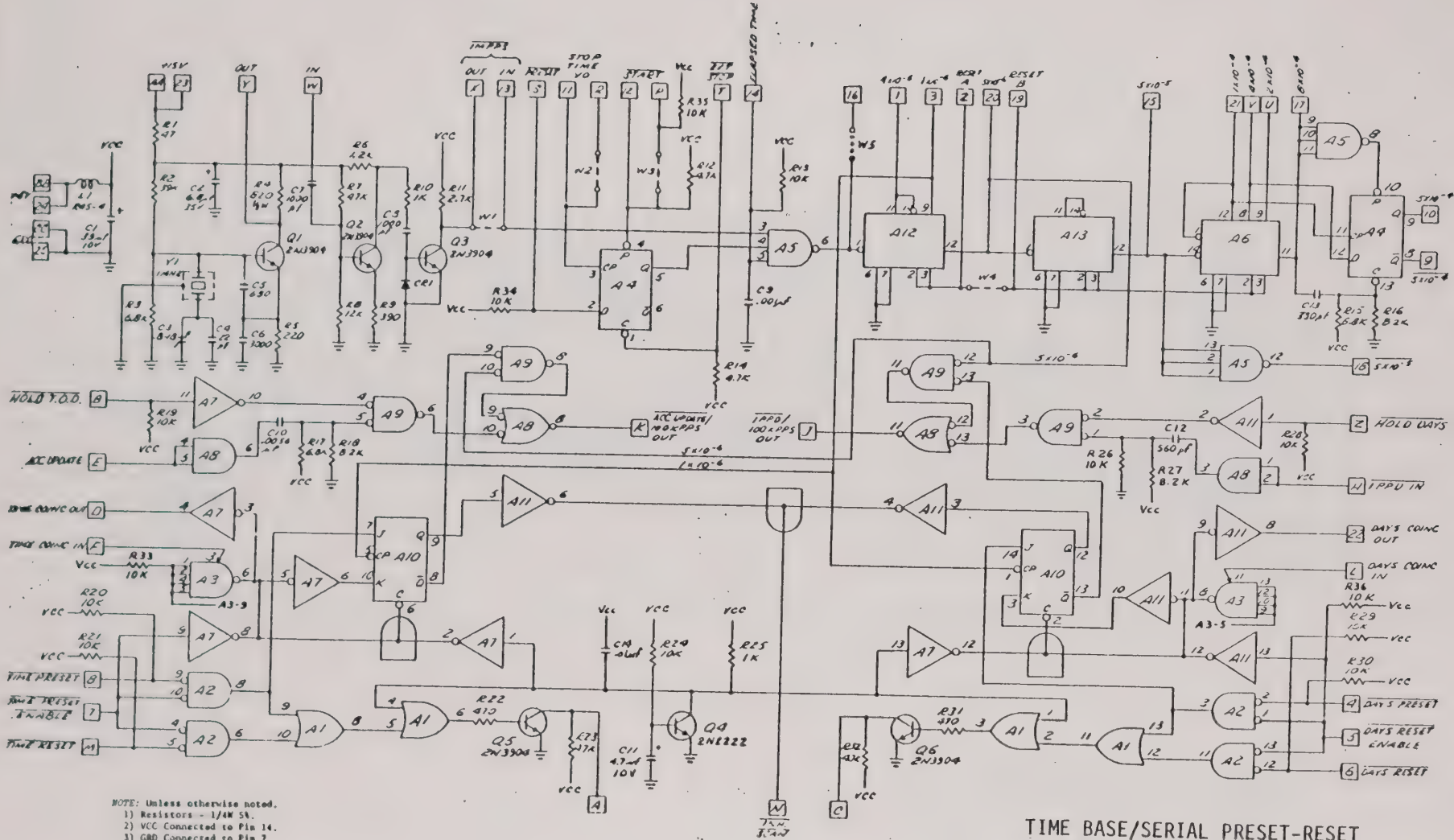
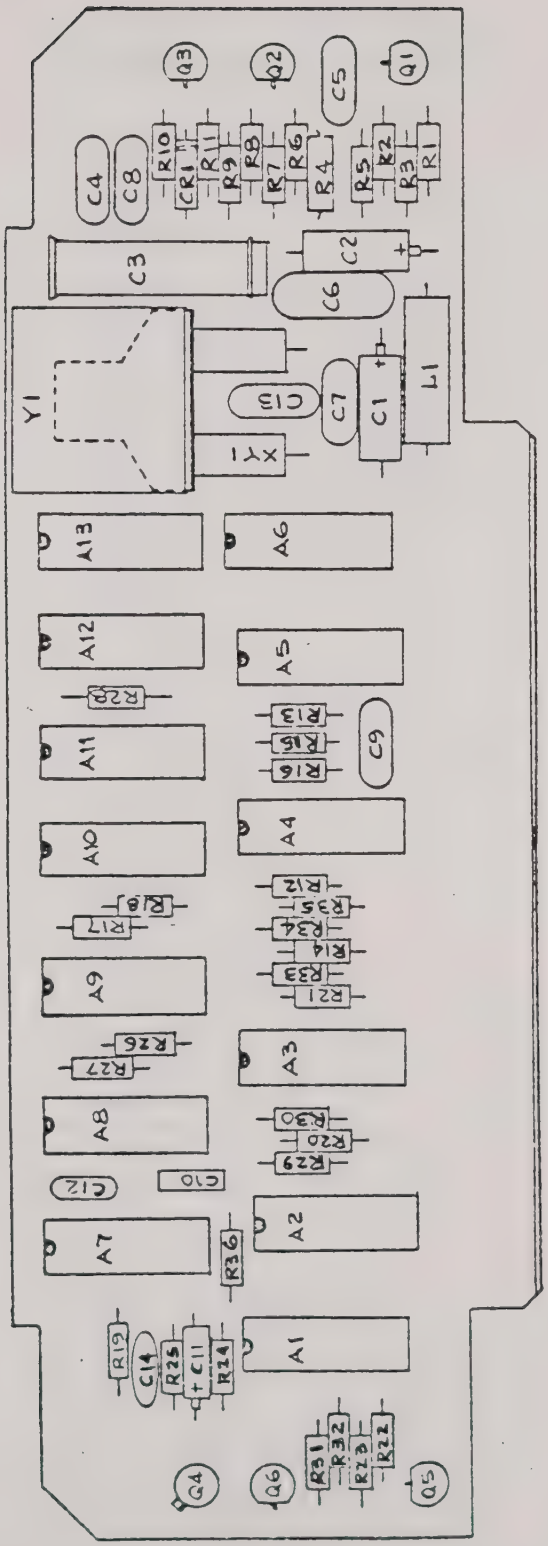


NOTE: Unless otherwise noted.
1) Resistors - 1/4W 5%.
2) VCC Connected to Pin 14.
3) GRD Connected to Pin 7.
4) SN7432N - A1,A9
MC3002P - A2
SN15-830N - A3
SN7410N - A5
SN7474N - A4
SN7490 - A6,A12,A13 (VCC to Pins, GRD to Pin 10)
MC836P - A7,A11
SN7408N - A8
SN7473N - A10 (VCC to Pin 4, GRD to Pin 11)

TIME BASE/SERIAL PRESET-RESET
SCHEMATIC #021566-7-11 REV B_1



TIME BASE AND SERIAL PRESET
ASSEMBLY #021566-4-11 REV B1

PARTS LIST

TIME BASE SERIAL PRESET/RESET #021566-7-11 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly	021566-4-11
	Schematic	021566-7-11
A1	Integrated Circuit, SN7432N	045257
A2	Integrated Circuit, MC3002P	025739
A3	Integrated Circuit, SN15830N	019712
A4	Integrated Circuit, SN7474N	025241
A5	Integrated Circuit, SN7410N	019706
A6	Integrated Circuit, SN7490N	025732
A7	Integrated Circuit, MC836P	025704
A8	Integrated Circuit, SN7408N	103093
A9	Same as A1	
A10	Integrated Circuit, SN7473N	019709
A11	Same as A7	
A12	Same as A6	
A13	Same as A6	
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 6.8 µF, 35 V	100182
C3	Capacitor, .8-18 pF, Variable	100102
C4	Capacitor, 22 pF	100068
C5	Capacitor, 680 pF	100275
C6	Capacitor, 3000 pF	100149
C7	Capacitor, 1000 pF	100243
C8	Same as C7	
C9	Capacitor, .001 µF	100076
C10	Capacitor, .0056 µF	116056
C11	Capacitor, 4.7 µF, 10V	100205
C12	Capacitor, 560 pF, DM	100222
C13	Capacitor, 330 pF	100276
C14	Capacitor, .01 µF, Disc	100103
CR1	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1-3	Transistor, 2N4124	101377
Q4	Transistor, 2N2222	101347
Q5,6	Same as Q1	
R1	Resistor, CC 47 Ω 5%, 1/4W	101560
R2	Resistor, CC 39 k 5%, 1/4W	101561
R3	Resistor, CC 6.8 k 5%, 1/4W	101544
R4	Resistor, 820 Ω 5%, 1/4W	101656
R5	Resistor, 220 Ω 5%, 1/4W	101566

PARTS LIST

TIME BASE SERIAL PRESET/RESET #021566-7-11 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R6	Resistor, CC 1.2 k 5%, 1/4W	101581
R7	Resistor, CC 47 k 5%, 1/4W	101574
R8	Resistor, CC 12 k 5%, 1/4W	101565
R9	Resistor, CC 390 Ω 5%, 1/4W	101592
R10	Resistor, CC 1 k 5%, 1/4W	101569
R11	Resistor, CC 2.7 k 5%, 1/4W	101599
R12	Resistor, CC 4.7 k 5%, 1/4W	101599
R13	Resistor, CC 10 k 5%, 1/4W	101570
R14	Same as R12	
R15	Same as R3	
R16	Resistor, CC 8.2 k 5%, 1/4W	101595
R17	Same as R3	
R18	Same as R16	
R19	Same as R13	
R20	Same as R13	
R21	Same as R13	
R22	Resistor, CC 470 Ω 5%, 1/4W	101625
R23	Same as R12	
R24	Not Used	
R25	Same as R10	
R26	Same as R13	
R27	Same as R16	
R28	Same as R13	
R29	Same as R13	
R30	Same as R13	
R31	Same as R22	
R32	Same as R12	
XY1	Socket, Crystal	100769
Y1	Crystal, 1 MHz	102450
	Extractor	100865

CIRCUIT DESCRIPTION
AGC/CYCLE DETECTOR
SCHEMATIC #021569-7-1

1) GENERAL

The AGC/Cycle Detector card contains two separate and independent circuits. The first circuit (AGC) provides automatic gain control for the incorming signal. The second circuit (Cycle Detector) generates 3 control signals: Upper Large Cycle, (ULC); Lower Large Cycle, (LLC); and Each Cycle (EC).

2) AGC

Serial time-code input (from the tape unit, or other source), pin 19, is applied to a voltage divider network which consists of R12 and FET Q1. The bias on the gate of Q1 determines the ratio of the divider network and therefore the signal level at the gate of Q2. Q2 is a source follower providing high input impedance (so as not to load the divider network) and low impedance to drive differential amplifier A5. The input to A5 is applied to the "+" input (pin 3) via C10 for noninverting operation, (or to the "-" input, pin 2 via R39 for inverting operation, as applicable to the particular circuit configuration.)

A5 is provided with negative feedback through R20 for a maximum gain of about 40 dB, and two "roll-off" networks C13-R22, and C12 to ensure stability. Pins T,Y and A are normally connected by an external jumper. When optional filter networks are used, they are connected between pins T and Y.

The amplified signal is applied to the base of Q4 which controls the emitter voltage of Q3. Q4 and Q3 form a signal peak-detection circuit which provides the AGC control voltage to the gate of Q1. The output on pin T is set from 2 to 2.5 V p-p through the AGC potentiometer R4.

3) CYCLE DETECTOR

The output of amplifier A5 is also applied to 3 cycle-detector circuits A1,A2 and A3.

A1 triggers at the zero-axis crossing and will generate a square wave at the input carrier frequency. The hysteresis of this trigger circuit is adjustable by means of the EC ADJ potentiometer, R25.

A2 and A3 generate output pulses only upon receipt of the Large Half Cycle, A2, the ULC and A3 the LLC.

These 2 amplifiers will initiate their signals when the input signal reaches about 75% of the LHC amplitude and will terminate them when the input signal reaches zero. The trigger points are adjustable by means of the ULC ADJ and LLC ADJ potentiometers R29 and R34.

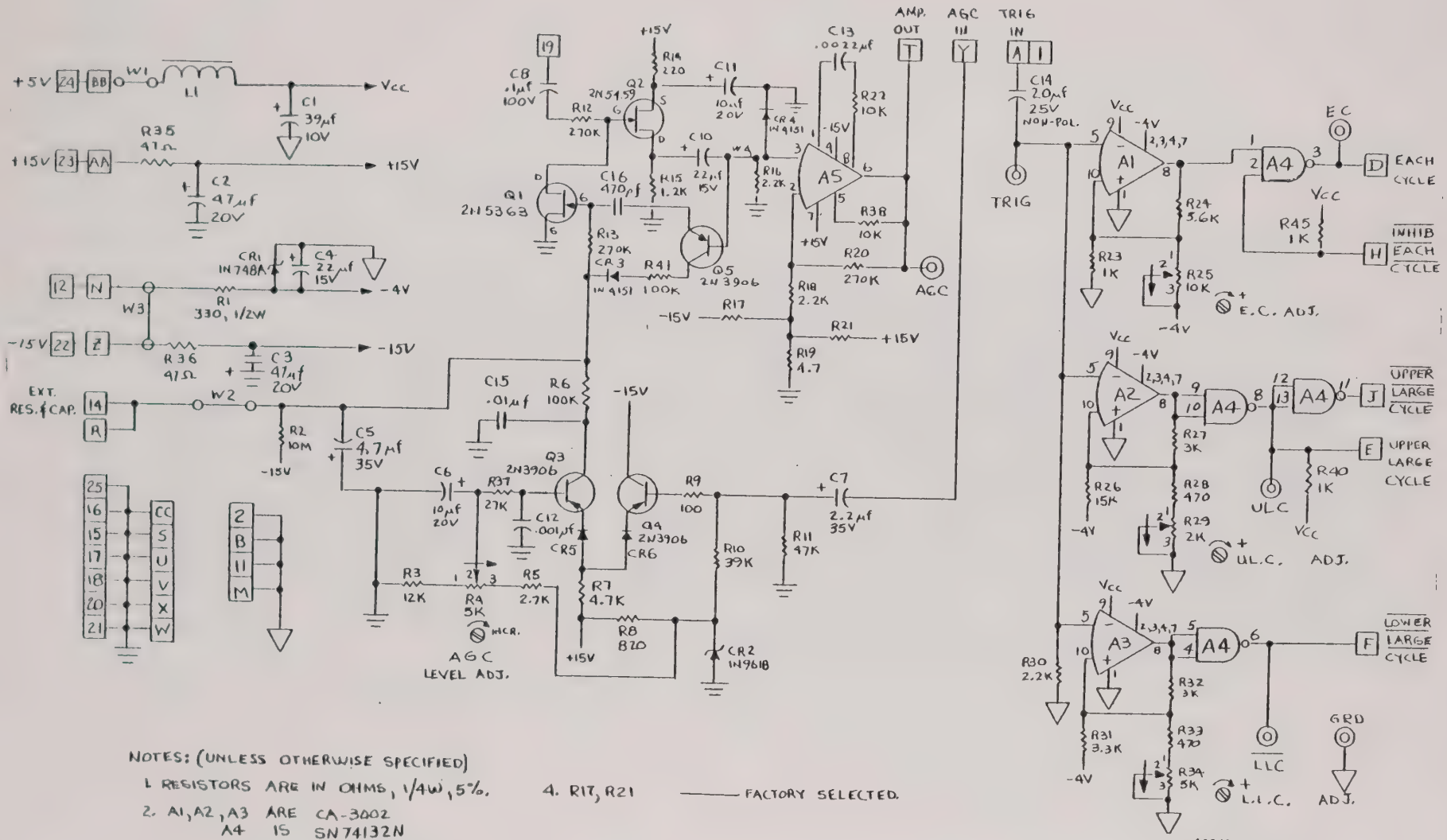
Saturating logic amplifiers, A4-2, A4-4 and A4-6, serve to amplify, invert the signals, and to provide isolation. A4-8 and A4-12 are used to inhibit the EC output when the $\overline{\text{INH EC}}$ (pin H) is grounded.

During normal operation of the Generator, the preset circuits connect the normal update inputs to their respective accumulators. In the case of the TOD Preset circuit this is the 1 pps input to pin E which is buffered by A8-6 then differentiated and fed to the TOD Accumulator through A9-6, A8-8 and pin K.

To initiate a TOD Preset cycle the $\overline{\text{Enable}}$ input to pin 7 must be at ground. (This condition exists in the PRESET position of the MODE Switch.) A ground on pin 7 opens gates A2-6 and A2-8 and removes the clear input to flip-flop A10-9 through inverter A7-8. The actual preset cycle is started when the PRESET/RESET Switch is momentarily thrown to the PRESET position grounding pin 8. The A2-8 output goes positive enabling the J input to flip-flop A10-9 and resetting the TOD Accumulator through A1-8, A1-6, Q5 and pin A. The next negative transition of the 500 kpps (1×10^{-6}) clock input sets flip-flop A10-9 and opens gate A9-8 to the 100 kpps (5×10^{-6}) pulse train feeding these signals to the TOD Accumulator update input through A8-8 and pin K.

5) RESET OPERATION

The accumulator is reset to zero when power is first turned on in the system. This occurs in the interval before capacitor C11 charges turning on Q4. The TOD Accumulator may also be reset when pin 7 is at ground by momentarily grounding pin M.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. A1, A2, A3 ARE CA-3002
   A4 IS SN74132N
   A5 IS MC-1439G
3. PIN 14 OF A4 IS CONNECTED TO Vcc
   " 7 " " " " " GRD.
4. R17, R21 ——— FACTORY SELECTED.

AGC/CYCLE DETECTOR
SCHEMATIC #21569-7-1 REV S

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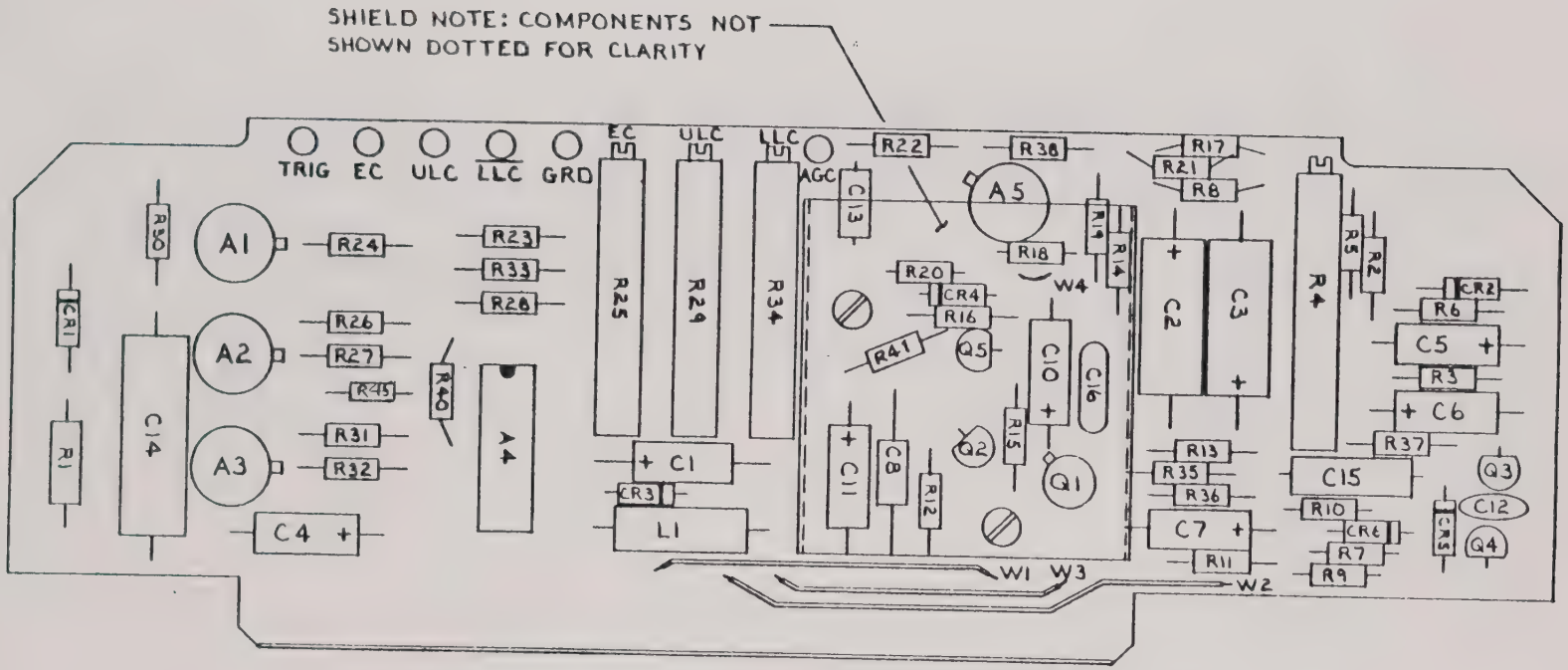


AGC/CYCLE DETECTOR ASSEMBLY #21569-4-1 REV N

PARTS LIST

AGC/CYCLE DETECTOR #021569-7-1 (REV U)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021569-4-1
	Schematic	021569-7-1
A1-3	Integrated Circuit, CA3002	025701
A4	Integrated Circuit, SN74132	025270
A5	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 47 µF, 20 V	100186
C3	Same as C2	
C4	Capacitor, 22 µF, 15 V	100125
C5	Capacitor, 4.7 µF, 35 V	100071
C6	Capacitor, 10 µF, 20 V	100063
C7	Capacitor, 2.2 µF, 35 V	100100
C8	Capacitor, .1 µF, 100 V	100141
C9	Not Used	
C10	Same as C4	
C11	Same as C6	
C12	Capacitor, 1000 pF, Disc	100076
C13	Capacitor, .0022 µF	100185
C14	Capacitor, 20 µF, 25 V	100264
C15	Capacitor, .01 µF, 200 V	100168
C16	Capacitor, 470 pF, Mica	100283
CR1	Diode, IN748A	100384
CR2	Diode, 1N961B	100395
CR3-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5363	101403
Q2	Transistor, 2N5459	101384
Q3-5	Transistor, 2N3906	101378
R1	Resistor, 330 Ω 5%, 1/2 W	101474
R2	Resistor, 10 M 5%, 1/4 W	101564
R3	Resistor, 12 k 5%, 1/4 W	101565
R4	Potentiometer, 5 k Beckman 78P	101938
R5	Resistor, 2.7 k 5%, 1/4 W	101599
R6	Resistor, 100 k 5%, 1/4 W	101558
R7	Resistor, 4.7 k 5%, 1/4 W	101598
R8	Resistor, 820 Ω 5%, 1/4 W	101567
R9	Resistor, 100 Ω 5%, 1/4 W	101609
R10	Resistor, 39 k 5%, 1/4 W	101561

PARTS LIST

AGC/CYCLE DETECTOR #021569-7-1 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R11	Resistor, 47 k 5%, 1/4 W	101574
R12	Resistor, 270 k 5%, 1/4W	101769
R13	Same as R12	
R14	Resistor, [illegible] k 5%,	101566
R15	Resistor, 1.2 k 5%, 1/4 W	101581
R16	Resistor, 2.2 k 5%, 1/4 W	101562
R17	Factory Select	
R18	Same as R16	
R19	Resistor, 4.7 Ω 5%, 1/4 W	101796
R20	Same as R12	
R21	Factory Select	
R22	Resistor, 10 k 5%, 1/4 W, CC	101570
R23	Resistor, 1 k 5%, 1/4 W, CC	101569
R24	Resistor, 5.6 k 5%, 1/4 W, CC	101584
R25	Potentiometer, 10 k, Beckman 78P	101918
R26	Resistor, 15 k 5%, 1/4 W, CC	101552
R27	Resistor, 3 k 5%, 1/4 W, CC	101548
R28	Resistor, 470 Ω 5%, 1/4 W, CC	101625
R29	Potentiometer, 2 k Beckman 78P	101876
R30	Same as R16	
R31	Resistor, 3.3 k 5%, 1/4 W	101569
R32	Same as R27	
R33	Same as R28	
R34	Same as R4	
R35	Resistor, 47 Ω 5%, 1/4 W	101560
R36	Same as R35	
R37	Resistor, 27 k 5%, 1/4 W	101587
R38	Same as R22	
R39	Not Used	
R39	Same as R23	
R40	Same as R23	
R41	Same as R6	
R42-44	Not Used	
R45	Same as R23	

CIRCUIT DESCRIPTION
READER LOGIC
SCHEMATIC #021588-7-3

1) GENERAL

Signals, $\overline{LLC}$ and EC respectively, are connected to pins A and 1 of the Reader Logic Card. The Reader Logic circuit accepts the EC and LLC signals and detects the ONES, ZEROS and MARKS in the code. These signals are used to shift the BCD time information of the input code into a shift register and then transfer it to the TOD Accumulator Card which drives the Display driver and Code Generator.

2) FUNCTIONAL

The basic scheme is as follows:

When a MARK is detected, the 9-bit shift register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" counter (A10) is advanced one.

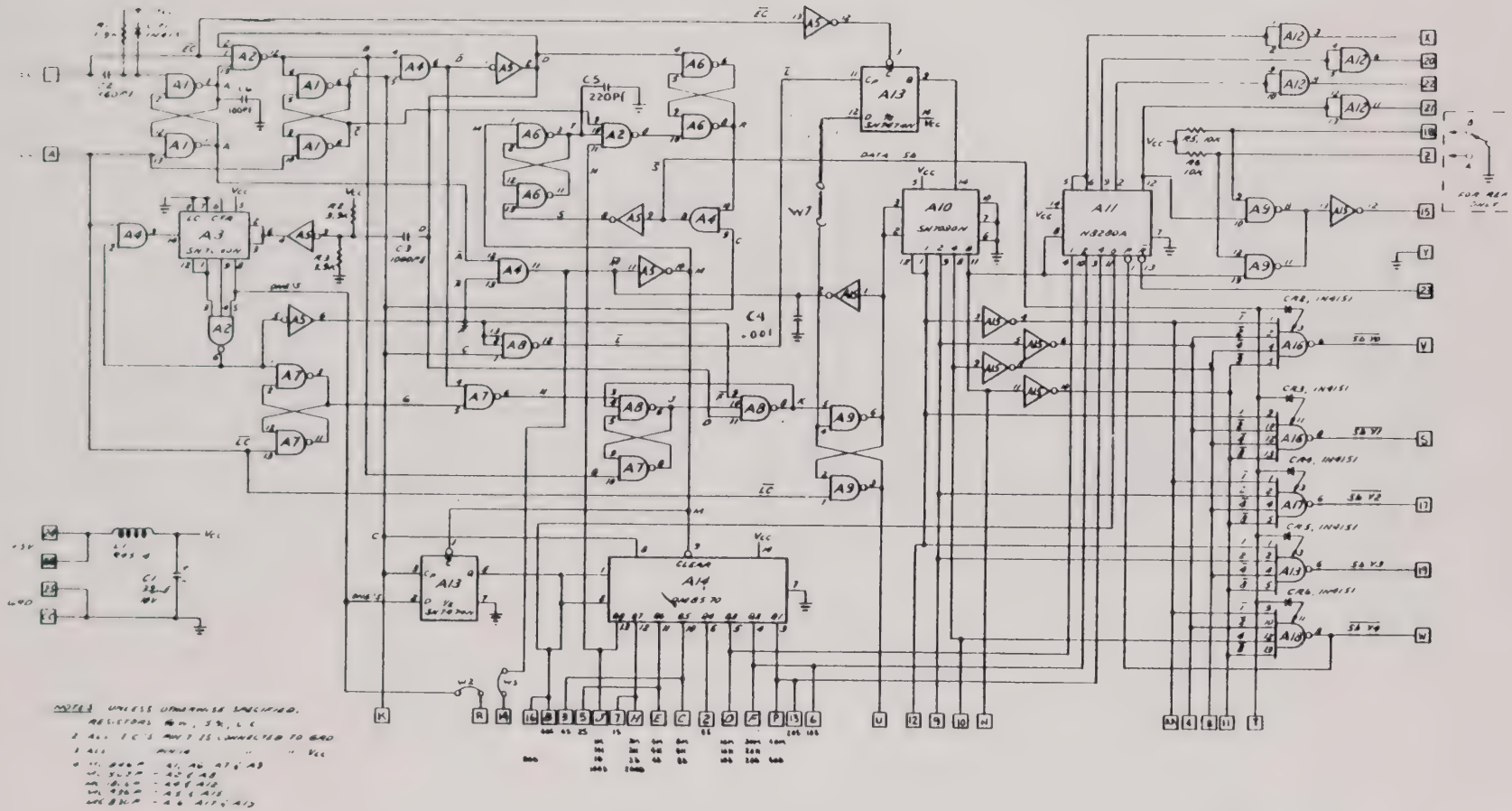
When the second MARK of the double MARK is detected, the sequence is changed so that the "Y" counter is set to ZERO if it was not already at ZERO. The "Y" counter is not advanced for this MARK, nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the TOD Accumulator.

When the next MARK is detected, the register is cleared, a ONE entered, and the "Y" counter advanced one. After 9-bits are shifted into the register, the information is transferred to the minutes section of the TOD Accumulator. This cycle of operation is repeated a third time for hours information. If Days Option E20 is included, two additional cycles transfer this information to the Days Accumulator. The "Y" counter continues to count MARKS throughout the time frame.

When the first MARK of the next double MARK is detected, it steps the "Y" counter from 9 to zero, advancing the TOD Accumulator one second. It is thus, updated at the beginning of the frame, and will contain the same information (assuming no errors) scanned-in during the frame.

The readout does not change during the scan-in, since the TOD Accumulator is already updated.

The serial level shift code at pin R is fed to the Error Bypass circuit where it is compared with the output from the Code Generator which represents, in serial form, the contents of the Time Accumulator.



READER LOGIC SCHEMATIC #021588-7-3 REV D

PARTS LIST

READER LOGIC #021588-7-3 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly	021588-4-3
	Schematic	021588-7-3
A1	Integrated Circuit, MC846P	019716
A2	Integrated Circuit, MC862P	019719
A3	Integrated Circuit, SN7090N	025732
A4	Integrated Circuit, MC1806P	025733
A5	Integrated Circuit, MC836P	025704
A6	Same as A1	
A7	Same as A1	
A8	Same as A2	
A9	Same as A1	
A10	Same as A3	
A11	Integrated Circuit, N8380A	025722
A12	Same as A4	
A13	Integrated Circuit, SN7474N	025241
A14	Integrated Circuit, DM8570	025751
A15	Same as A5	
A16-18	Integrated Circuit, MC830P	019712
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, Mica	100222
C3	Capacitor, .001 µF, DM15	100243
C4	Capacitor, .001 µF, Disc	100076
C5	Capacitor, 220 pF, DM15	100220
C6	Capacitor, 100 pF	100173
CR1-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W, CC	101601
R4	Not Used	
R5	Resistor, 10 k 5%, 1/4 W, CC	101570
R6	Same as R5	
W2,3,7	Wire, Insulated, 24 GA	
	Extractor	100865

CIRCUIT DESCRIPTION
FWD/REV CONTROL
SCHEMATIC #021625-7-1

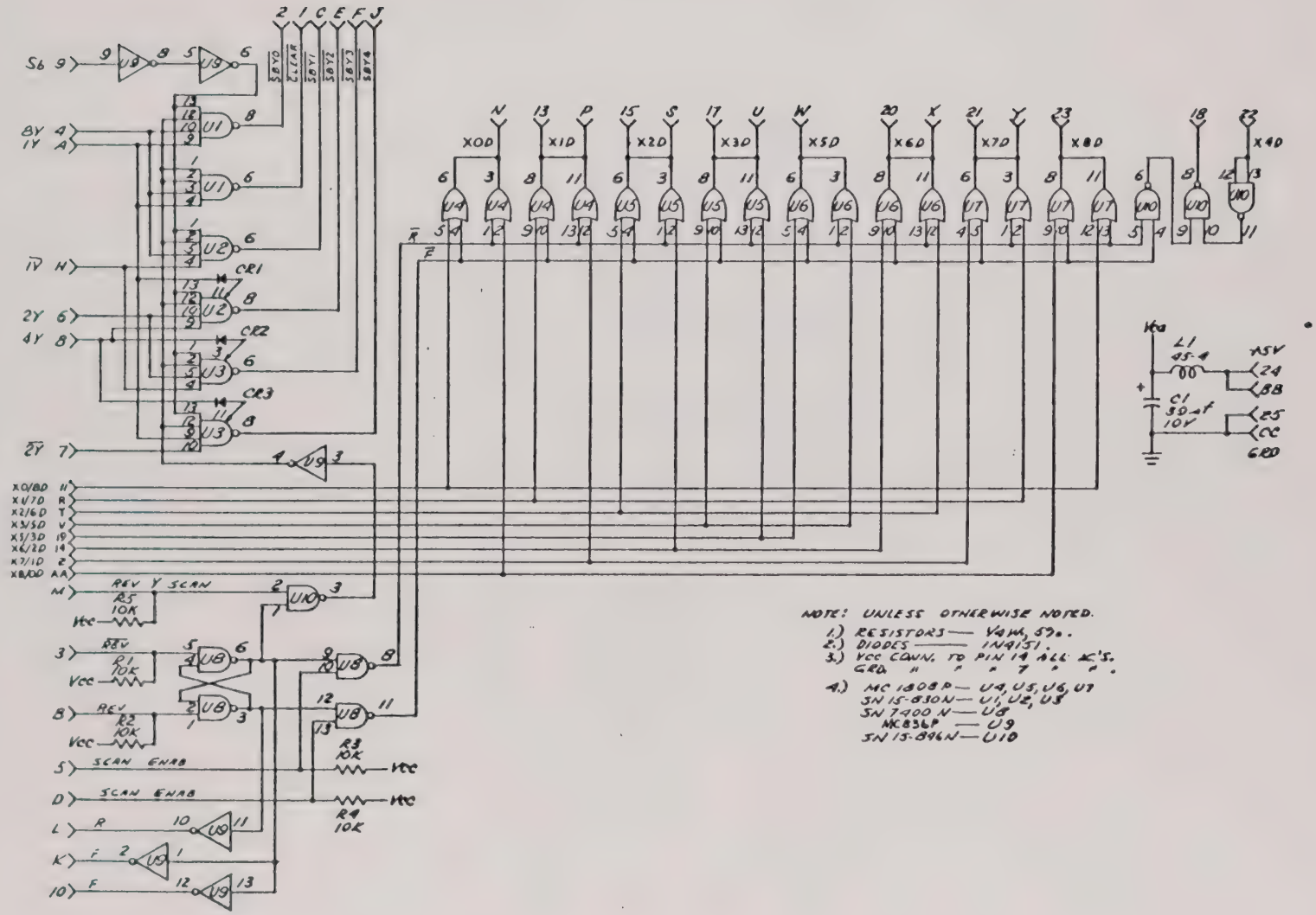
1) GENERAL

The FWD/REV Control Card, A13 contains gates which invert the order of the time data bits stripped from the input code when reading a reverse code. In addition, it provides buffered forward and reverse control signals and establishes the Y-Strobe signals needed to load data into the Time Accumulator when operating with a reverse code. This circuitry is active only when operating in one of the search modes. All circuits are disabled in the PRESET and GEN Modes.

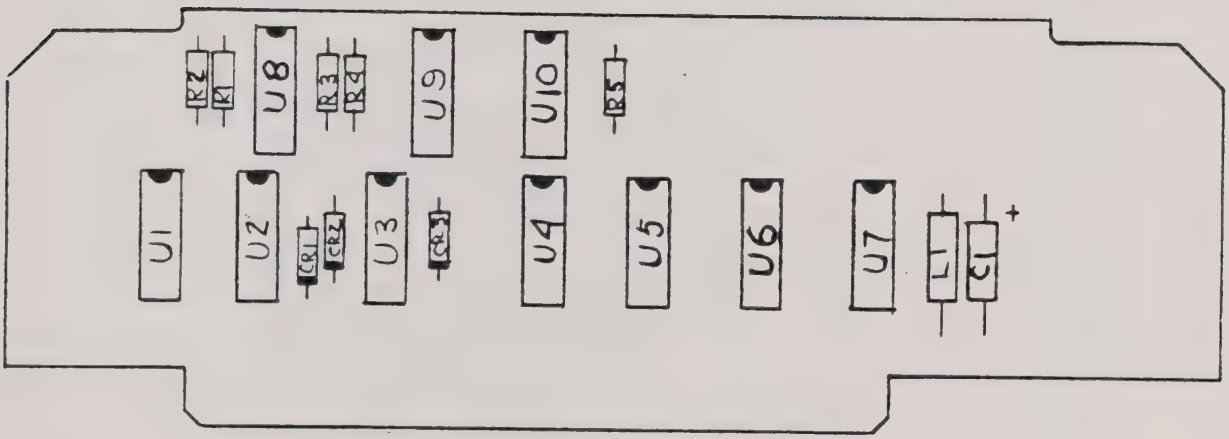
2) OPERATION

Referring to Schematic #021625-7-1, the FWD and REV signals from the Tape Search section are fed to pins 3 and B, respectively. When operating in reverse (tape transport moving in a reverse direction) the FWD (REV) signal is at ground, and the $\overline{\text{REV}}$ signal is positive. Flip-flop U8-6/3 is set. The positive output from U8-6 is fed to 4 circuits: 1) through U10-3 and U9-4, opening Y Strobe Scan gates U1,U2 and U3; 2) through U8-8, opening gates U4-3, U4-11, U5-3, U5-11, U6-3, U6-11, U7-3 and U7-11 to negative time data signals $\overline{\text{X0}}$ through $\overline{\text{X8}}$; 3) through U9-2 to the Error Bypass circuit, disabling forward Y Scan; and 4) through U9-12, clamping the Z-Rate signal at ground, thus blocking update of the TOD Accumulator (A15) and inhibiting operation of the Code Generator A17) and Modulator (A8) circuits. The Y Strobe Scan gates load the rearranged data bits into the TOD Accumulator (A15) as each frame is stripped from the input code.

When forward operation is established, flip-flop U8-6/3 is reset. The Y Strobe Scan gates are disabled (all outputs driven positive), gates U4-6, U4-8, U5-6, U5-8, U6-6, U6-8, U7-6 and U7-8 are open (time data restored to normal order); U9-12 and U9-2 outputs are up, restoring normal operation of the TOD Accumulator, Code Generator, Modulator and Error Bypass circuitry.


NOTE: UNLESS OTHERWISE NOTED.
1.) RESISTORS — ¼W, 5%.
2.) DIODES — 1N4151.
3.) Vcc CONN. TO PIN 14 ALL IC'S.
GRD. " " " 7 " " .
4.) MC 1809P — U4, U5, U6, U7
SN 15-830N — U1, U2, U3
SN 7400 N — U8
MC836P — U9
SN 15-896N — U10

FWD/REV CONTROL SCHEMATIC #021625-7-1 REV B



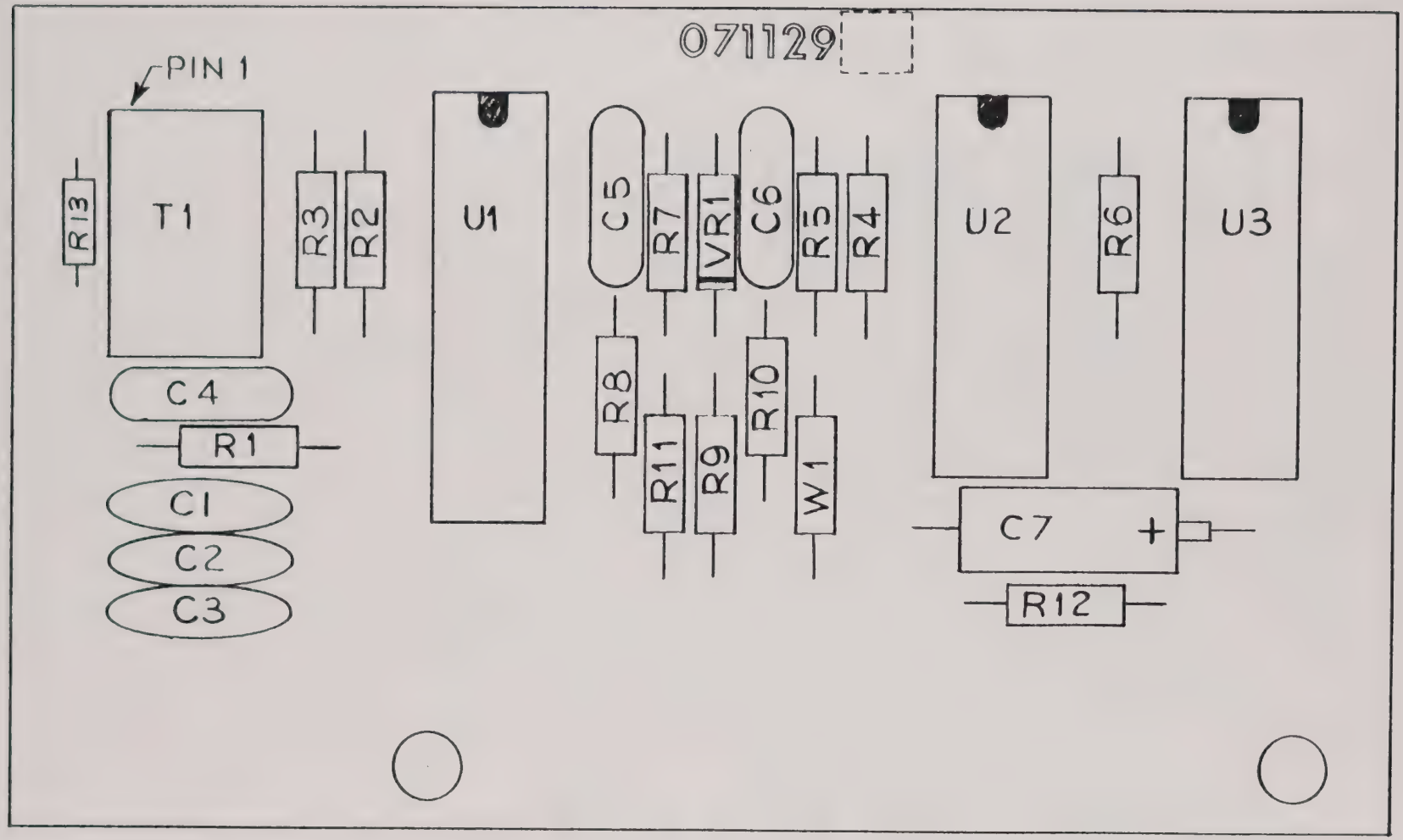
FWD/REV CONTROL ASSEMBLY #021625-4-1 REV A

PARTS LIST

HIGH STABILITY OSCILLATOR FOR OPTIONS B11 and B13

SCHEMATIC #7-071128-01

REF.	DESCRIPTION	SD PART NO.
	Assembly	07112801
	Schematic	7-07112801
A401-1	Assembly, PC	07112901
J402A	Connector, Shell Female 9 Position	102811
P201	Connector, Shell Male 5 Position	101263
P402A	Connector, Shell Female 9 Position	102811
Y1	Oscillator Modification	07113001
	Oscillator Chassis	071128
	Fastener Swage 90° 4-40 (1/16)	101090
	Spacer Modification	07113102
	Spacer Swage 6-32 x 1/4 (1/16)	100783
	Insulator	07113201
	Cable Clamp Saddle Type #4	07113201
	PHMS 4-40 x 3/8 Crescent	10062606
	Lockwasher Split #4 Crescent	100711
	Flatwasher #4 Crescent	100703
	THMS 6-32 x 3/8 Blk. Oxide	102775
	Shoulder Washer #6 Fiber	116076
	Oscillator 3 MHz	03342701
	Insulator	07113202
	Contact Pin	10282202
	Contact Pin Scoket	10282202



OSCILLATOR BOARD ASSEMBLY #07112901 REV B

PARTS LIST

OSCILLATOR BOARD #07112901

REF.	DESCRIPTION	SD PART NO.
	Assembly	07112901
	Schematic (Ref. Sch. Dwg. #7-07112801)	7-07112901
C1,2	Capacitor, .05 µF, 50 V	100134
C3	Capacitor, .005 µF, 150 V	100058
C4	Capacitor, 100 pF, 500 V	100173
C5,6	Capacitor, 1000 pF, 100 V	100243
C7	Capacitor, 39 µF, 10 V	100183
R1,2,4-6	Resistor, 10 k 5%, 1/4 W	101570
R3	Resistor, 39 k 5%, 1/4 W	101561
R7,11	Resistor, 47 k 5%, 1/4 W	101574
R8	Resistor, 120 k 5%, 1/4 W	101580
R9	Resistor, 47 Ω 5%, 1/4 W	101560
R10	Resistor, 1 k 5%, 1/4 W	101569
T1	Transformer	103227
U1	Integrated Circuit, CD4049AE	103217
U2	Integrated Circuit, DM8093	
U3	Integrated Circuit, SN7473N	019709
VR1	Diode, Zener 4.7 V	100388
W1	Jumper, Molded	102879

CIRCUIT DESCRIPTION
DAYS/ID (OPTION E13)
BLOCK DIAGRAM #7-061028

1) GENERAL

The days/ID Option is shown on the instrument Block Diagram. This option adds the #021632-7-21 Days Accumulator Card (A18), Preset thumbwheel switches S12-S14, Leap Year/ID switch S16, a colon and three-digit display to Display Assembly (A102) and the associated wiring.

Parallel BCD Days/ID outputs are supplied to connector J3, through buffers on the Days Accumulator Card. These 12-bits have the following specifications:

Code: 8-4-2-1

Logic: "1" = +5 ±0.5 V behind 6 kΩ.
"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

An ID Update input (IC levels) to rear panel BNC connector J13, is provided. This input is fed to a circuit on the Modulator Board (A20).

PARTS LIST
DAYS/ID (OPTION E13) #06131618 REV A

DESCRIPTION	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-06102806
A18	Assembly, Days Accumulator	021632-4-21
CR5	Lamp, LED	100455
CR6	Same as CR5	
J13	Connector, BNC	101155
S12	Thumbwheel	05130011
S13	Same as S12	
S14	Same as S13	
U7	Integrated Circuit, DD700	045203
U8	Same as U7	
U9	Same as U7	
V4	Display, SP353	102404
XA18	Connector, PC Edge	101204
	Card Guide	021340-1-2
	Insulator, BNC	100823
	Fiber Washer	101074
	Ground Lug, BNC	100495
	DELETE	
J13	Hole Plug, BNC	100952
S12	Switch Spacer	102358
S13	Same as S12	
S14	Same as S12	
S16	Cover Plate, Slide Switch	05120802

CIRCUIT DESCRIPTION
DAYS ACCUMULATOR
SCHEMATIC #021632-7-21

1) GENERAL

The Days Accumulator Card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

2) DECADE DIVIDERS

The up to three decade dividers are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10, A13 and A15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters A11.

4) INPUT INHIBIT CIRCUIT

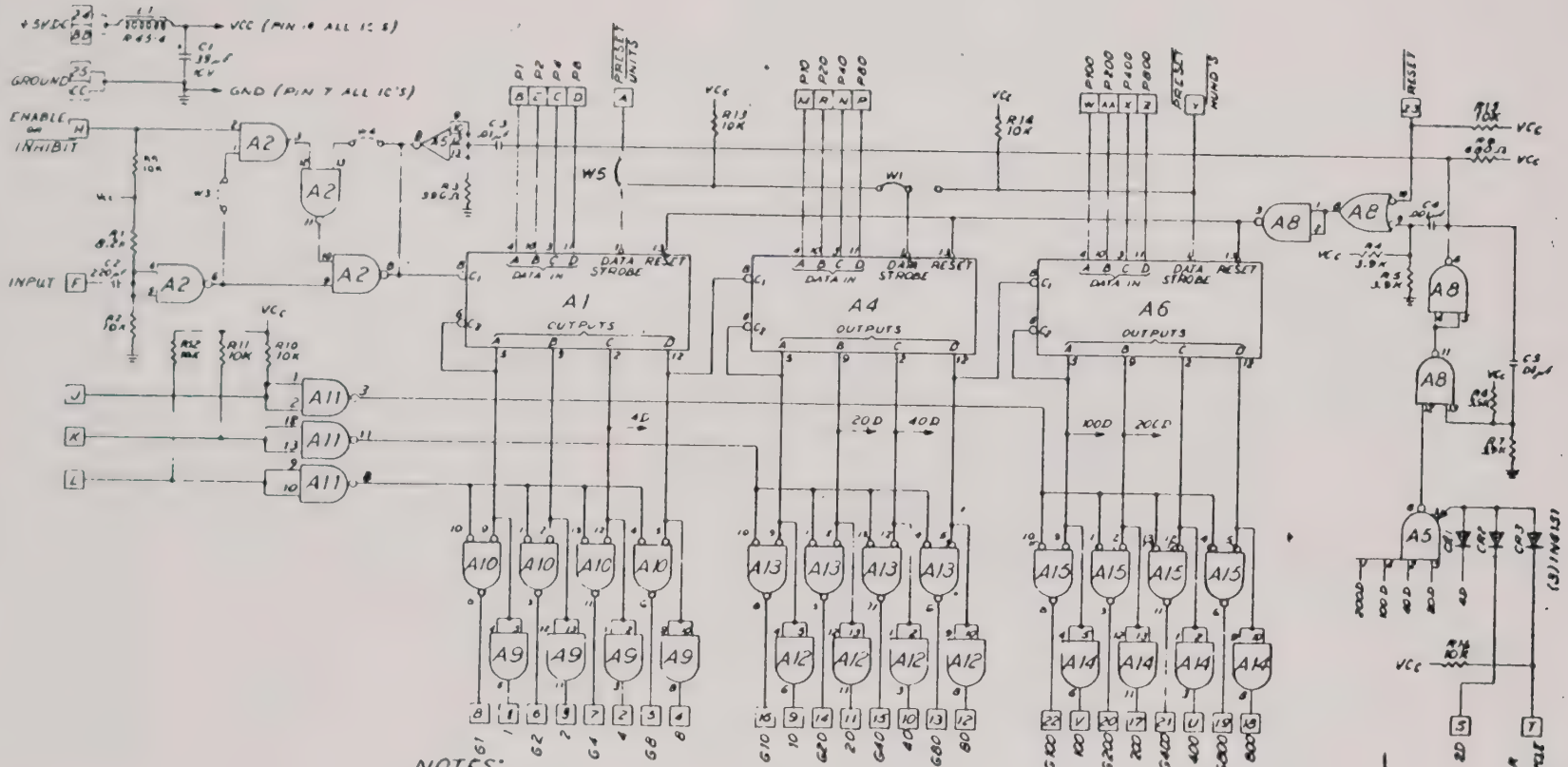
This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8, 11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) DAYS RECYCLE CIRCUIT

Gate 5-6 is a 4-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate seven inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the 2-day output. At the selected count, the output of A5-6 will go low, triggering one-shot A8-11, 6. The one-shot output is a negative-going pulse (from +5 to 0 V). The leading edge of the pulse (ac-coupled into A8-8) causes the three dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is ac-coupled into A5-8 where it is inverted and used to input one count to the first decade. The resulting accumulator contents are 001.

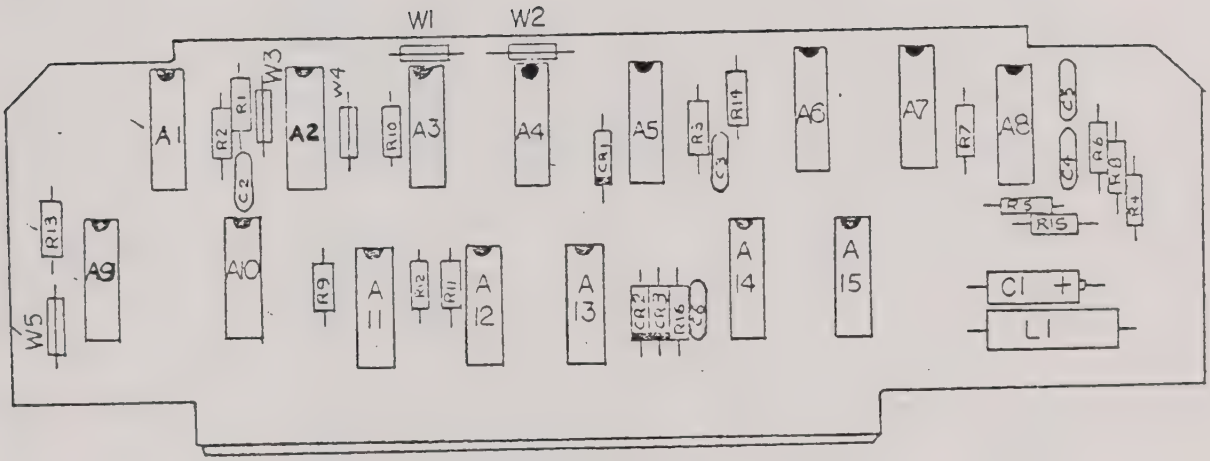
021632-7-21



NOTES:
1. INT. CKT. TYPES AS FOLLOWS:
A1, 4, 6 = NB280P.
A2 = MC846P
A5 = MC830P.
A8 = SN7400N.
A9, 12, 14 = MC1806P.
A10, 13, 15 = MC1808P.
A11 = MC846P.
2. C3 USED FOR DAYS RECYCLE TO "1".
3. FOR TENS TO PRESET WITH UNITS INSTALL W1 AND NOT W2.

DAYS ACCUMULATOR SCHEMATIC #021632-7-21 REV B

OPTION E13-4



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

DAYS ACCUMULATOR #021632-7-21 REV A

REF.	DESCRIPTION	SD PART NO.
	Assembly	021632-4-1
	Schematic	021632-7-21
A1	Integrated Circuit, N8280P	025722
A2	Integrated Circuit, MC846P	019716
A3	Not Used	
A4	Same as A1	
A5	Integrated Circuit, MC830P	019712
A6	Same as A1	
A7	Not Used	
A8	Integrated Circuit, SN7400N	019705
A9	Integrated Circuit, MC1806P	025733
A10	Integrated Circuit, MC1808P	025734
A11	Same as A2	
A12	Same as A9	
A13	Same as A10	
A14	Same as A9	
A15	Same as A10	
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF	100044
C3	Capacitor, .01 µF, Disc	100103
C4	Capacitor, .001 µF, Disc	100076
C5	Same as C3	
CR1	Diode, 1N4151	
CR2	Same as CR1	
CR3	Same as CR1	
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k 5%, 1/4 W	101595
R2	Resistor, 10 k 5%, 1/4 W	101570
R3	Resistor, 390 Ω 5%, 1/4 W	101592
R4	Resistor, 3.9 k 5%, 1/4 W	101601
R5	Same as R4	
R6	Same as R4	
R7	Same as R4	
R8	Resistor, 680 Ω 5%, 1/4 W	101669
R9	Same as R2	
R10	Same as R2	

PARTS LIST

DAYS ACCUMULATOR #021632-7-21 REV A (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R11	Same as R2	
R12	Same as R2	
R13	Same as R2	
R14	Same as R2	
R15	Same as R2	
R15	Same as R2	
R16	Same as R2	
W1	Jumper Molded	102879
W2	Not Used	
W3	Not Used	
W4	Not Used	
W5	Same as W1	
	Extractor	100865

CIRCUIT DESCRIPTION
MILLISECONDS (OPTION E14)
BLOCK DIAGRAM #7-061028

1) GENERAL

The Milliseconds Option is shown on the instrument Block Diagram. This option adds J6 and the associated wiring to the basic unit.

Parallel BCD Milliseconds outputs are supplied to connector J6 through buffers on the Minor Counter Card (A9). These 12-bits have the following specifications:

Code: 8-4-2-1

Logic: ""1" = +5 ±0.5 V behind 6 kΩ.

"0" = +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

OPTIONS S11 and S11A
SYNCHRONIZATION

1) EXTERNAL SYNCHRONIZATION - Option S11

Option S11 is available with Systron-Donner 8100 Series Digital Clocks and Time Code Generators. This option provides the capability of automatically starting the clock or generator in sync with an external pulse. Starting accuracy to within one µs can be expected, exclusive of sync pulse rise time delay. The option also includes the capability of advancing and retarding the clock time at precise rates to allow re-synchronization without the need to interrupt time accumulation.

When Option S11 is added, the following changes are incorporated in the basic instrument:

1. A rear panel BNC connector is added to accept the external start command.
2. A front panel BNC connector is added to allow access to the internal 1 pps pulse for comparison purposes.
3. A front panel Auto/Manual start control is added.
4. Front panel controls are added to select the advance/retard rate and direction.

2) SPECIFICATIONS

EXTERNAL START PULSE: A positive going level change of +4.5 V, minimum, for a duration of not less than 5 µs. Input impedance is 10 kΩ. Up to 50 V may be applied without damage.

1 pps OUTPUT: 0 to +5 V (nominal) pulse from a 6 kΩ source. Width is 100 ms. Leading edge is "on time".

ADVANCE/RETARD RATES: 1 usec/sec., 10 usec/sec., 100 usec/sec., 1 msec/sec., 10 msec/sec., 100 msec/sec.

3) WWV SYNCHRONIZATION - Option S11A

Option S11A provides the same capability as Option S11 and, in addition, allows full synchronization to radio stations WWV in Fort Collins, Colorado, and WWVH in Puunene, Maui, Hawaii. Option S11A includes:

1. A filter and shaper to extract the 5 ms "tick" from the WWV audio signal.
2. A tick lamp to provide a visual indication of the quality of tick reception and an "on time" light to indicate coincidence between the WWV tick and the internal, delayed 1 pps in the clock. Front panel thumbwheel switches to automatically correct the transmission propagation delays from 00.0 to 99.9 ms.
3. Advance/Retard control for resynchronization.

All controls for synchronization are located on the front panel as are the tick and on-time lights. A front panel BNC connector allows access to the combined WWV tick and the internal delayed 1 pps signals to allow resynchronization with a single trace oscilloscope.

4) SPECIFICATIONS

EXTERNAL START PULSE: Same as Option S11.

WWV SYNC INPUT: Unit will detect the WWV (1 kHz) or WWVH (1.2 kHz) second ticks with a minimum input level of 0.5 V rms.

PROPAGATION DELAY: Three thumbwheel switches allow inserting a compensation for propagation delays of up to 99.9 ms in 0.1 msec. increments.

ADVANCE/RETARD RATES: Same as Option S11.

5) START UP PROCEDURE FOR EXTERNAL SYNCHRONIZATION OPTION S11A

EQUIPMENT REQUIRED:

1. WWV Receiver: Tick Output; 0.5 V rms, minimum.
2. Oscilloscope: Vert: 0.5 V/div, 100 kHz bandwidth, minimum.

   Horiz: 0.5 to 5 mS/div. (Oscilloscope required only when precision must be better than +3 mS.)

No requirement is required (other than the start pulse source itself) for the EXT start mode.

SETUP:

1. Connect the Tick output of the receiver to the "WWV IN" BNC on the rear of the Time Code Generator (TCG).
2. Adjust the tick output of the receiver for about 3 V p-p (1.5 V p-p minimum). This will correspond to about 1 V p-p on the TICK and PED BNC.

MILLISECONDS SYNCHRONIZATION:

START-UP:

1. Note that the TICK lamp is flashing once each second.
2. Set the 3 PROPAGATION DELAY switches (XX.X ms) to the calculated time required for the signal to propagate from the transmitter to the receiver.
3. Place the mode switch of the TCG in HOLD position.
4. Momentarily position the START switch to MANUAL.
5. Place the mode switch of the TCG in the STOP position for a minimum of one second.
6. Position the mode switch to HOLD.
7. Make certain that a good clean tick signal is present; then position the START switch to AUTO and hold for one second.
8. The TCG is now synchronized to within +10 mS*. Synchronization using an ON TIME lamp or scope may be performed for greater accuracy.

SYNCHRONIZATION USING ON TIME LAMP:

1. Position the PER SEC switch to 1 ms.
2. Hold the ADV/RET switch in the RET position until the ON TIME lamp stops flashing.
3. Hold the ADV/RET switch in the ADV position until the ON TIME lamp flashes and then stops flashing; note how many flashes this requires.

*Any uncertainty in the propagation delay time must be added on these figures.

4. Hold the ADV/RET switch in the RET position for one-half the number of flashes counted in this position less two.

5. Synchronization is now accurate to within +2 mS.*

SYNCHRONIZATION USING A SCOPE:

1. Connect the vertical input of the scope (0.5/div and 2 mS/div) to the TICK and PED BNC on the front panel of the TCG.

2. Observe the pedestal and tick on a common baseline.

3. Select a convenient rate on the PER SEC switch and, using the ADV/RET switch, superimpose the tick and the pedestal as shown in Figure 1.

4. Return the PER SEC switch to OFF.

5. Synchronization is now accurate to within +100 μs*.

SETTING TIME-OF-DAY REGISTER:

1. Choose a convenient time about one minute in the future and set the time-of-day preset thumbwheel switches to this time.

2. Momentarily position the TOD PRESET/RESET switch to PRESET.

3. During the one second interval immediately preceeding the time set in the above sentence, position the TCG mode switch to GEN.

4. Observe the time display and determine if it is now correct. If it should be one second late, return the mode switch to HOLD and repeat these four steps.

SETTING DAYS/ID NUMBER REGISTER (for instruments equipped w/Option E13).

1. Set the desired day or ID number into the DAYS/ID thumbwheel switches.

2. Momentarily position the DAYS/ID PRESET/RESET switch to PRESET.

USE OF THE EXT. START INPUT:

A pulse (see specifications) may be applied to the EXT START input and used in place of the WWV tick.

NOTE

The TICK and ON TIME lamp are not used in the EXT. START mode.

1. The propagation delay switches may be used if applicable; if not, set them to 00.00.

2. Position the TCG mode switch to STOP for one second, minimum.

METHOD #1

1. Position the mode switch to HOLD.

2. Position the START switch to AUTO and hold it until the next start pulse occurs.

3. Set the time-of-day as in the first step of Setting Time-of-Day Register.

4. Set the days/ID number (if applicable).

METHOD #2

1. Preset the time-of-day register to the time of the start pulse as done in Setting Time-of-Day Register.

*Any uncertainty in the propagation delay time must be added on these figures.

PARTS LIST

RWD/REV CONTROL #021625-7-1 REV A

REF.	DESCRIPTION	SD PART NO.
	Assembly	021625-4-1
	Schematic	021625-7-1
C1	Capacitor, 39 µF, 10 V	100183
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-5	Resistor, 10 k 5%, 1/4 W	101570
U1-3	Integrated Circuit, SN15830N	019712
U4-7	Integrated Circuit, MC1808P	025734
U8	Integrated Circuit, SN7400N	019705
U9	Integrated Circuit, SN15846N	025704
U10	Integrated Circuit, SN15846N	019716
	Extractor	

CIRCUIT DESCRIPTION
MINOR COUNTER
SCHEMATIC #021632-7-2

1) GENERAL

The Minor Counter Card A9, can provide up to 3 serial decades with common reset, parallel preset and 2-sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. Provision is included for 3 output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2) DECADE DIVIDERS

The up to 3 decade dividers (A1, A4, A6) are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. ONe of the 2 sets (A10, A13 and A15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters on A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A208 forma an RS flip-flop.

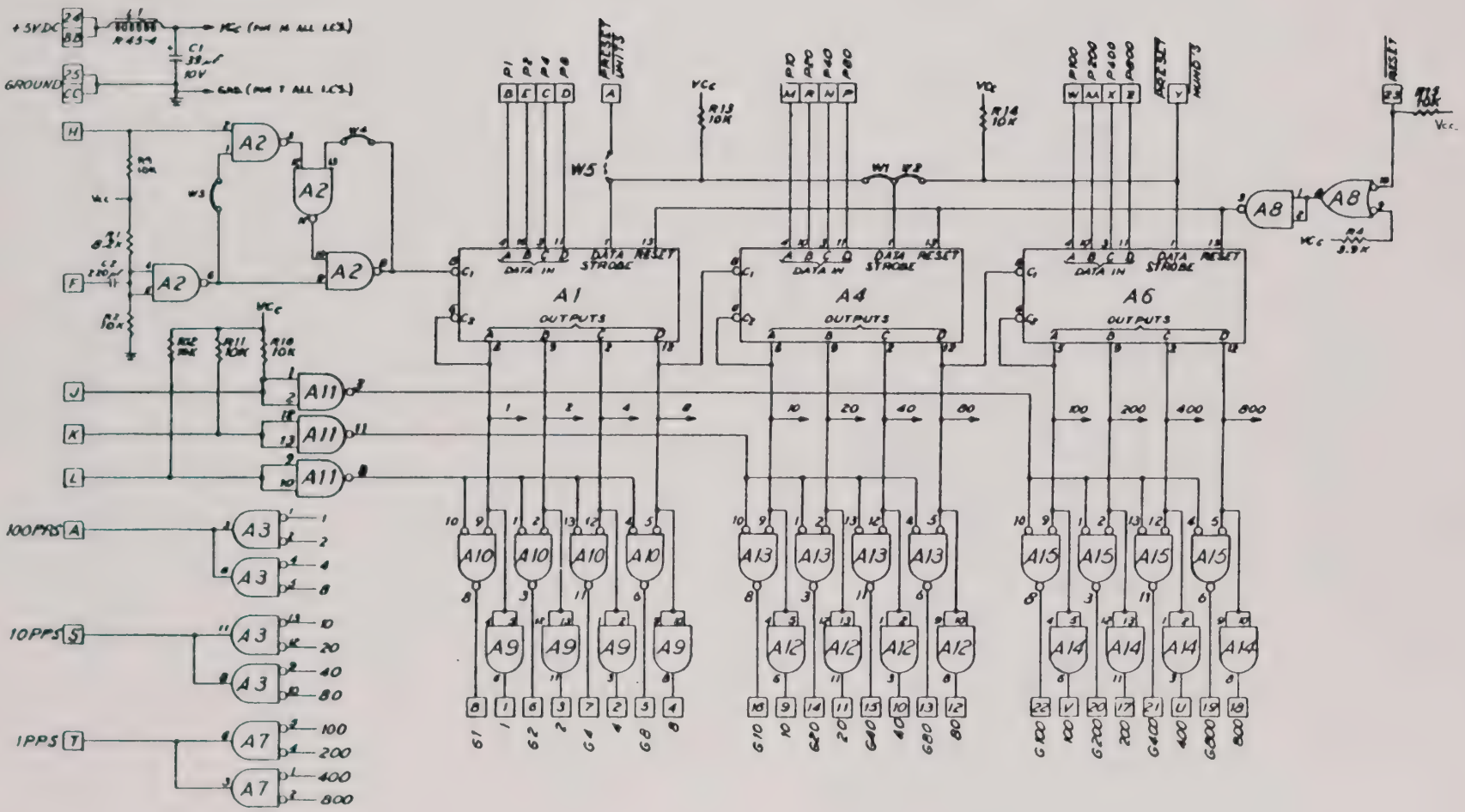
A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating flip-flop A2-8/11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) OUTPUT PULSE RATES

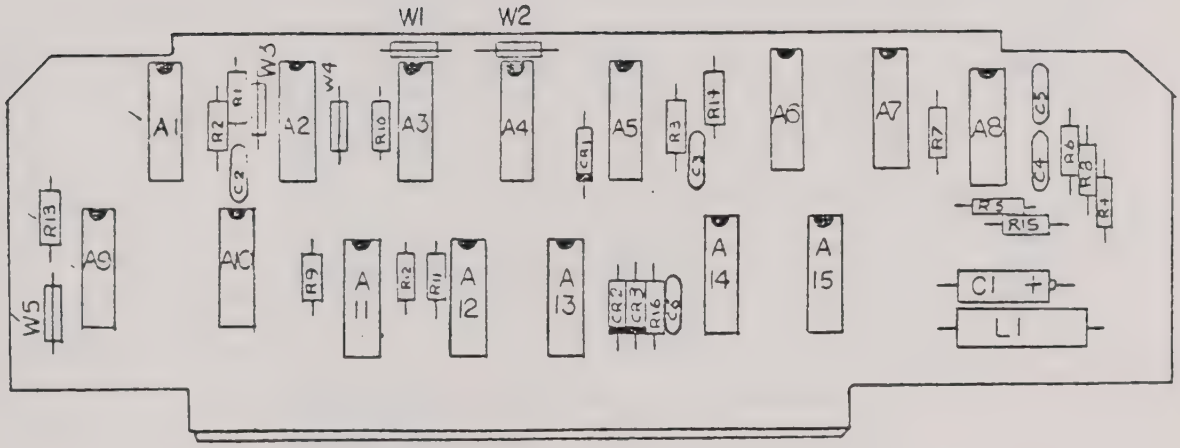
Three sets of gates are used to produce three 10%-duty-cycle pulse rates. Each pulse goes high when the 4 outputs from the ocrresponding decades are low (leading edge on time). The pulse remains up until the output of the decade is 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 6 kΩ.

The pulse rate outputs are fed to pins A, S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 (see assembly #021632-4-1) is removed when the rate outputs are supplied.

8152-7-79



MINOR COUNTER SCHEMATIC #021632-7-2 Rev B



MINOR COUNTER ASSEMBLY #021632-4-1 Rev C

PARTS LIST

MINOR COUNTER #021632-7-2 REV D

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #031632-4-1)	021632-4-2
	Schematic	021632-7-2
A1	Integrated Circuit, N8280A	025722
A2	Integrated Circuit, MC846P	019716
A3	Integrated Circuit, MC1810P	025735
A4	Same as A1	
A5	Not Used	
A6	Same as A1	
A7	Same as A3	
A8	Integrated Circuit, SN7400N	019705
A9	Integrated Circuit, MC1806P	025733
A10	Integrated Circuit, MC1808P	025734
A11	Same as A2	
A12	Same as A9	
A13	Same as A10	
A14	Same as A9	
A15	Same as A10	
C1	Capacitor, 39 µF, 10 V, Tant	100183
C2	Capacitor, 220 pF, 500 V	100220
L1	Inductor, R45-4	
R1	Resistor, 8.2 k 5%, 1/4 W, CC	101595
R2	Resistor, 10 k 5%, 1/4 W, CC	101570
R3	Not Used	
R4	Resistor, 3.9 k 5%, 1/4 W, CC	101601
R5-8	Not Used	
R9-15	Same as R2	
	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
PRESET AND ERROR BYPASS
SCHEMATIC #7-05153802

1) GENERAL

This card contains Preset Control, Error Bypass, Pulse Rate, Z-Rate, FWD/REV, and Reset circuits. It is used in the Model 8132 Reader, the Model 8134 Reader/Search Unit, the Model 8152 Generator/Reader and the Model 8154 Generator/Reader/Serach unit.

2) OPERATION

PRESET CONTROL: Referring to the lower right corner of the schematic, Preset Logic is provided for detecting TOD and Days Coincidence in the Model 8154 Time Code Generator/Reader/Search Unit. When armed in the PRESET Mode, these circuits combined with the comparator, detect coincidence between the time entered on the front panel PRESET/START TIME thumbwheel switches and the contents of the accumulator. The coincidence signals are sent to preset control circuits on Time Base & Control Card A27. When Days/ID Option E13 is included, these circuits separate the Days and TOD sections of the comparator providing separate Days and TOD Coincidence outputs to Card A27.

ERROR BYPASS: The Error Bypass circuit is shown at the top of the schematic. It is enabled in the READ Forward Mode of Operation only and includes provision for selecting 0,3,5,7 or 9 frames of Error Bypass. This means that data stripped from the input code will not be loaded into the Accumulator until after the selected number of consecutive error frames has been counted. (READ Reverse is equivalent to "0" error bypass in which all data are loaded into the Accumulator irrespective of errors.)

The Error Bypass circuit accepts the serial level shift output from the Reader Logic Card and compares it with the serial level shift output from the Code Generator Card in exclusive OR gate U13-11. The output from this gate is fed to gate U7-6 along with blanking and sampling signals which differ as a function of the code being read and the options present in the Reader.

The sampling signal from U14-2 is developed in Counter/Decoder U1/U2 from the Z-Rate input and selected by U3. It is a pulse at Z4 time for IRIG and NASA Codes and at Z5 time for XR3 Code.

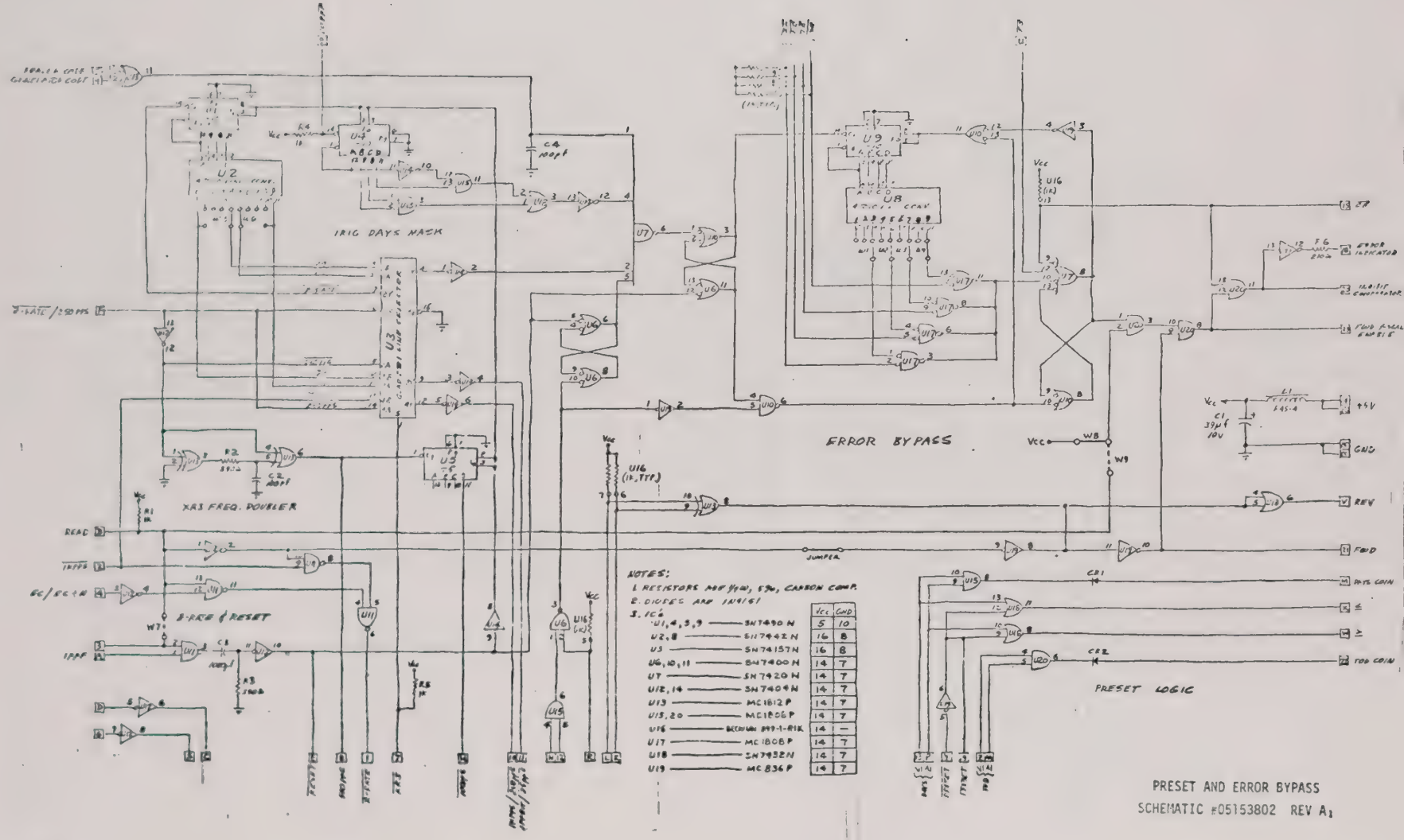
The IRIG Days Mask from U14-12 is developed by Counter U4 and associated decoding gates from the 20 ppF input to pin 9. It inhibits comparison of days bits so that readers without the Days Option can read IRIG Codes containing days.

The blanking signal from flip-flop U6-6, 8 restricts comparison to that portion of the code containing time information. It is set by the differentiated leading edge of the 1 ppF input through U11-3, C3, U12-10 ($\overline{\text{RESET}}$), and cleared by the output from the 3 input NAND gate formed from U15-6 and U6-3. The $\overline{\text{RESET}}$ signal clears flip-flop U10-3/U6-11, provided it was set by the detection of at least one error (U7-6 output going low) during the previous frame. Assuming that no error has occured, this flip-flop will not be set and output U6-11 will be high opening gate U10-6. When the cl clear signal from U6-3 occures during the current frams, it is inverted by U19-2 and fed through U10-6 resetting counter U9 and flip-flop U7-8/U10-8. The low output from U7-8 is fed through U20-3 and U20-8 to pin 23 and the Reader Logic Card, inhibiting forward Y-Scan. (Gates U20-3, 8 are open in READ Forward only.) This same

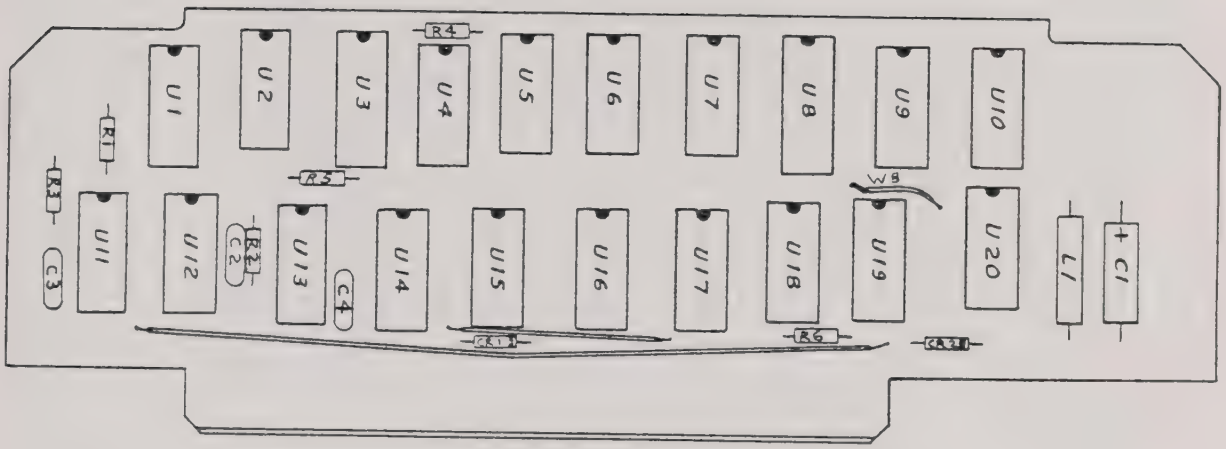
signal is fed through U20-11 to pin 20. The resulting output is used to enable the comparators in tape search units. Now, if an error occurs during the next frame, flip-flop U10-3/U6-11 will be set (with U10-3 high and U6-11 low) and, when U6-3 output goes low during the frame, U10-6 will be closed and counter U9 will not be reset. The RESET signal at the start of the next frame clears flip-flop U10-3/U6-11 and counter U9 accumulates one count. If the next frame is good, U9 is reset and the count starts over. If the next frame is bad, however, U9 accumulatoes a second count. The BCD outputs from counter U9 are decoded by U8 and fed to a set input to flip-flop U7-8/U10-8 through gates on U17 which are used to select the desired number of error bypass frames. When counter U9 reaches this number, flip-flop U7-8/U10-8 is set enabling forward scan of the time data (stripped from the input code by the Reader Logic during the next frame) into the Accumulator. The tape search comparators, when present, are inhibited by the output from U20-11 during this one frame. Counter U9 is reset through U19-4 and U10-11 and the sequence starts again. The selected number of consecutive error frames must occur before the input time data is permitted to be loaded into the Accumulator.

PULSE RATES: Selected pulse rates from U3 through U14-4 and U14-6 and from edge detector U13-3,6 and counter U5 are provided as outputs when XR3 Time Codes are being read.

Z-RATE and RESET: These circuits, shown at the lower left on the schematic, select Z-Rate output for GENERATE and READ and develope a RESET pulse from the leading edge of the 1 ppF input.



PRESET AND ERROR BYPASS
SCHEMATIC #05153802 REV A1



PRESET AND ERROR BYPASS ASSEMBLY #05153802 REV A_1

PARTS LIST

PRESET AND ERROR BYPASS #05153802 REV A_2

REF.	DESCRIPTION	SD PART NO.
	Assembly	05153802
	Schematic	7-05153802
C1	Capacitor, Tant 39 µF 10%, 10V	100183
C2	Capacitor, DM 100 pF 5%, 500V	100173
C3	Capacitor, DM 1000 pF 5%, 100V	100243
C4	Same as C2	
CR1	Diode, Signal 1N4151	100385
CR2	Same as CR1	
R1	Resistor, CC 1 k 5%, 1/4W	101569
R2	Resistor, CC 390 Ω 5%, 1/4W	101592
R3	Same as R2	
R4	Same as R1	
R5	Same as R1	
R6	Resistor, CC 270 Ω 5%, 1/4W	101542
U1	Integrated Circuit, SN7490N	025732
U2	Integrated Circuit, SN7442N	025749
U3	Integrated Circuit, SN74157N	045242
U4	Same as U1	
U5	Same as U1	
U6	Integrated Circuit, SN7400N	019705
U7	Integrated Circuit, SN7420N	025713
U8	Same as U2	
U9	Same as U1	
U10	Same as U6	
U11	Same as U6	
U12	Integrated Circuit, SN7404N	025779
U13	Integrated Circuit, MC1812P	025736
U14	Same as U12	
U15	Integrated Circuit, MC1806P	025733
U16	Integrated Circuit, Resistor Module 899-1-R1K	116454
U17	Integrated Circuit, MC1808P	025734
U18	Integrated Circuit, SN7432N	045257
U19	Integrated Circuit, MC836P	025704
U20	Same as U15	
W8	Wire, Jumper	
	Extractor	100855

CIRCUIT DESCRIPTION
POWER SUPPLY
SCHEMATIC #041810-7-9

1) GENERAL

The power supply provides four regulated dc voltages (±5V and ±15V), five unregulated dc voltages (±9V, ±21V and +210V), and an 18V rms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current-limited and are short-circuit-proof to ground. (Note: Overheating may result if a short is maintained over an extended period of time.) Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wir wired to provide regulation at the load. Fuses are provided for the unregulated +21V and +210V on the Power Supply Assembly.

Input power is 115/230V, 48 to 440 Hz at less than 100W with nominal line and all outputs fully loaded. (Note: The line frequency may be limited, 48 to 62 Hz unless Option L12 is utilized, by the fan characteristics if a fan is included in the unit.) Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 select switch, S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115V operation and in series for 230V operation. Selection is made by 115/230 switch, S101. (Note: Units are normally shipped in the 115V configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230V operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9V, one for ±21V and 18 Vrms, and the third for +210V.

2) NONREGULATED SUPPLIES

The +210V nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1,R2 and C5. The resulting output is fed through F2 (0.125A) to P103, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rated at 100 mA.

The ±21V nonregulated supplies are developed by bridge rectifier CR1 through CR4 and filtered by C1,C2,C8 and C11. The +21V output is used internally as the source for the +15V regulator. It is fed through F3 (1A) to P103, pins 15 and S, where it is available for use as a relay supply. The -21V output is used internally as the source for the -15V regulator, and to power both the -15V and -5V regulator amplifiers. It is also available at P103, pin 4, for external use. Each of the ±21V supplies is rated at 0.5A.

The 18 Vrms is derived from the secondary winding which provides the ac voltage to develop the ±21V. This rms voltage is fed through R15 to P103 pins 22 and Z.

The +9V nonregulated supply is developed by full-wave rectifier CR11, CR12 and filtered by C3, C4 and C10. It is used internally as the source for the +5V regulator, and to power both the -15V and -5V regulator amplifiers. It is available at P103 pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

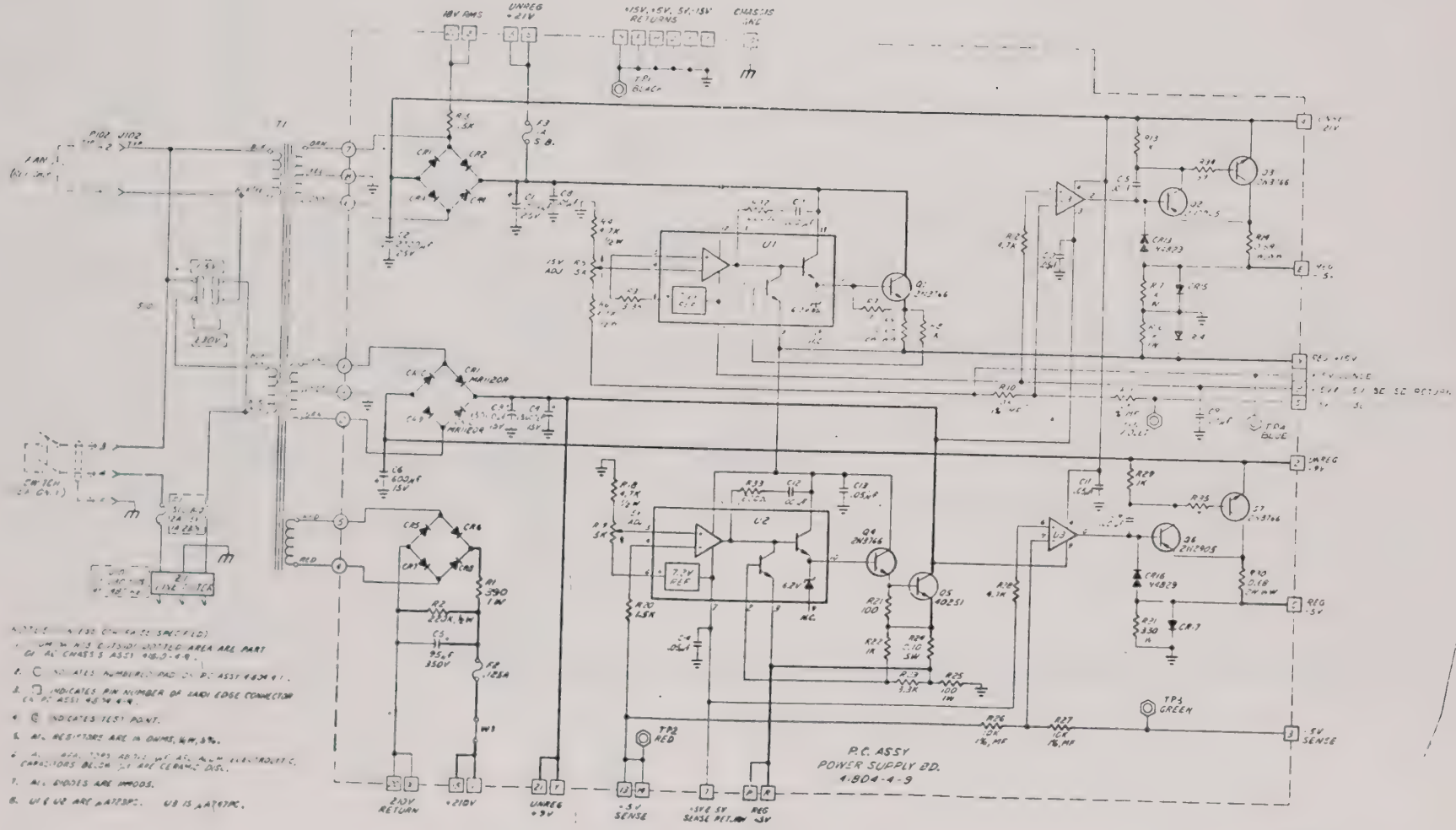
The -9V nonregulated supply from Full-wave rectifier CR9, CR10 and filter C6 is used internally as the source for the -5V regulator. It is available at P103, pin 2, for external use. It is rated at 0.5A.

3) REGULATED SUPPLIES

The regulated +15V, 0.5A output at P103, pin N, is established through pass transistor Q1 under the control of regulator U1 and the divider network (R4,R5,R6) between the +15V SENSE line (P103, pin 12) and ground. The voltage on the arm of 15V ADJ potentiometer (R5) is fed to U1 where it is compared with the internal reference, referred to the ±15V sense-return line (P103, pin 8). The current limit is imposed by sensing the drop across R9 and the circuit is stabilized by network R32,C7.

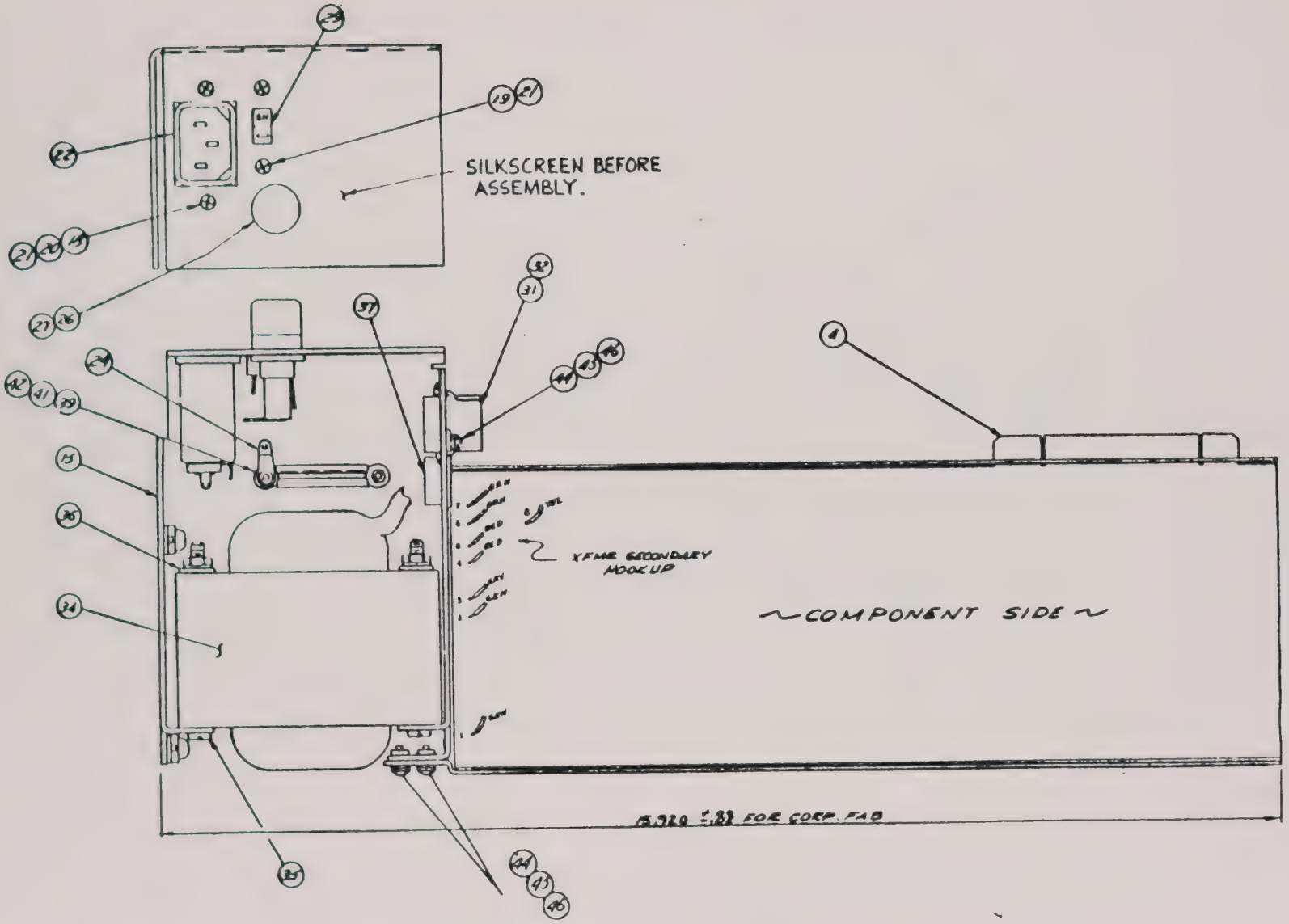
The regulated -15V, 0.5A output at P103, pin 5, is established through Q2 and Q3 under the control of regulator amplifier U3-12. It uses the +15V SENSE line as the reference, comparing it with the output through R10,R11 and the -15V supply. Potentiometer R5 serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 where the drop across R14 approaches one diode drop.

The regulated +5V, 5A output at P103, pins P and R, is established through Q4 and Q5 under the control of regulator U2 and a divider network (R18,R19). The +5V SENSE line at P103, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5V ADJ potentiometer (R19). The current limit is imposed by sensing the drop across R24 through divider R22,R23. The circuit is stabilized by network R33,C12. The regulated -5V, 0.5A output at P103, pin C, is established through Q6 and Q7 under the control of regulator amplifier U3-10. It uses the +5V SENSE line as reference, comparing it with the output through R26,R27 and the -5V SENSE line at P103, pin 3. The -5V output tracks the +5V supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches one diode drop.



POWER SUPPLY
SCHEMATIC #041810-7-9 REV C1

8152-7-79



POWER SUPPLY ASSEMBLY #041810-4-9 REV A

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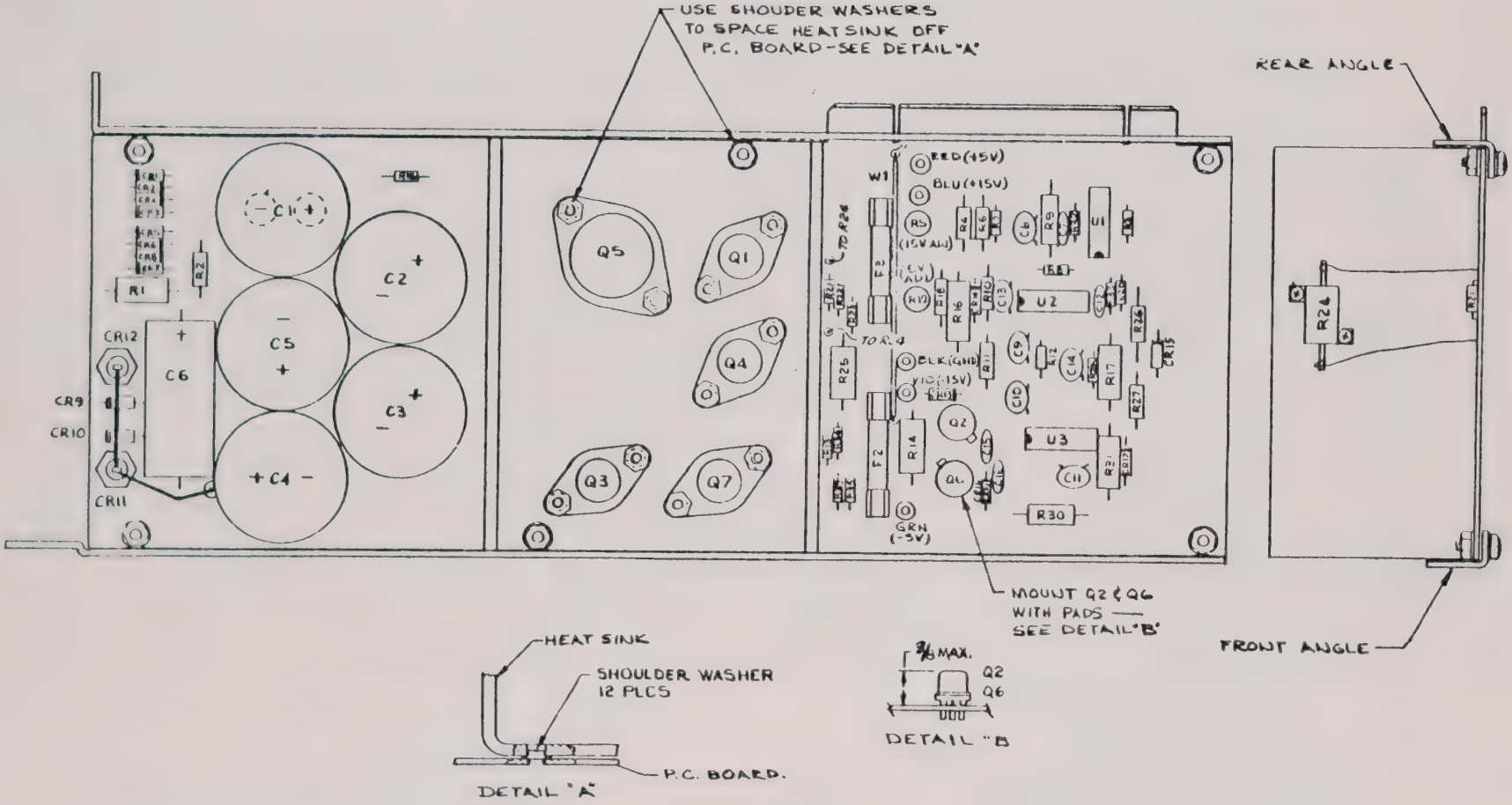
PARTS LIST

POWER SUPPLY ASSEMBLY #041810-4-9 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly, Power Supply	041810-4-9
	Assembly, Power Supply Board	041804-4-9
	Schematic, Power Supply	041810-7-9
F1	Fuse, 2A Slo-Blo 115V	100585
J101/Z1	Line Filter/Power Input	102461
J102	Connector, 5 positive receptacle shell	101264
S101	Switch, Slide 115/230	102331
T1	Transformer, Power	021408-6-1
XF1	Fuse, Post	102409
	Strip, Terminal 4 point	100084
	Cable, Power Supply	041810-3-6
	Chassis, AC	041810-1-6



POWER SUPPLY BOARD ASSEMBLY # 041804-4-9 REV C

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 REV E_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	041804-4-9
	Schematic	041810-7-9
C1	Capacitor, 2700 µF, 25V	100232
C2	Same as C1	
C3	Capacitor, 13000 µF, 15V	116070
C4	Same as C3	
C5	Capacitor, 95 µF, 350V	100259
C6	Capacitor, 600 µF, 15V	100258
C7	Capacitor, Disc .001 µF, 1 kV	100076
C8-11	Capacitor, .05 µF, 50V	100134
C12	Same as C7	
C13	Same as C8	
C14	Same as C8	
C15	Same as C7	
C16	Same as C7	
CR1-10	Diode, Signal 1N4005	100413
CR11	Diode, MR1120R	100424
CR12	Same as CR11	
CR13	Diode, 1N4829	100443
CR14	Same as CR1	
CR15	Same as CR1	
CR16	Same as CR13	
CR17	Same as CR1	
F1	Not Used	
F2	Fuse, Slo-Blo 3AG, 1A	100592
F3	Fuse, 3AG .125A	100584
Q1	Transistor, 2N3766	101373
Q2	Transistor, 2N2905	101382
Q3	Same as Q1	
Q4	Same as Q1	
Q5	Transistor, 40251	101354
Q6	Same as Q2	
Q7	Same as Q1	
R1	Resistor, CC 390 k 5%, 1W	101532
R2	Resistor, CC 220 k 5%, 1/2W	101458
R3	Resistor, CC 3.3 k 5%, 1/4W	101559
R4	Resistor, CC 4.7 k 5%, 1/4W	101511
R5	Resistor, Variable 5 k	101859
R6	Same as R4	
R7	Resistor, CC 1 k 5%, 1/4W	101569
R8	Same as R7	

PARTS LIST

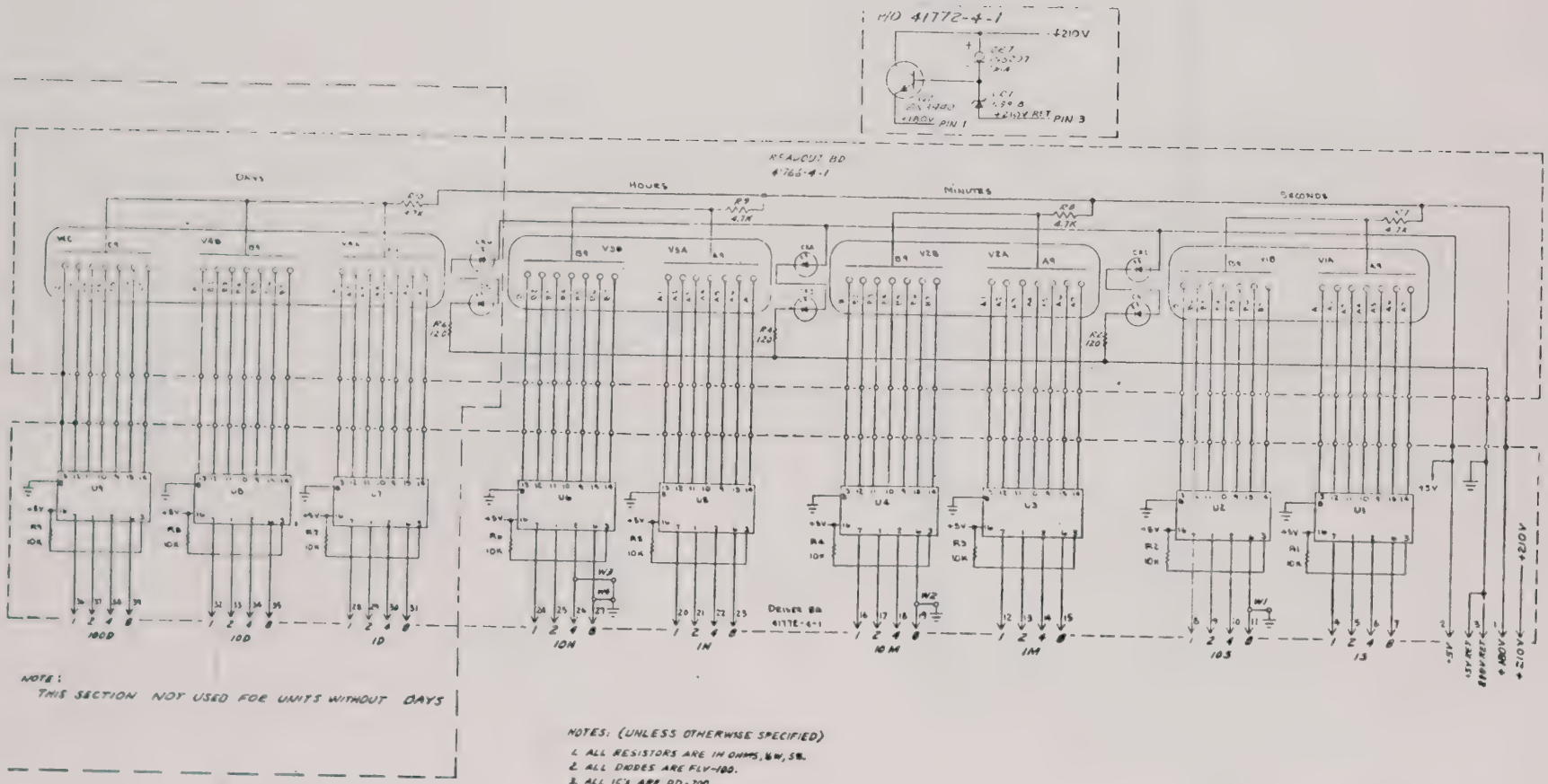
POWER SUPPLY BOARD #041804-4-9 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R9	Resistor, WW .68 Ω 2W	101829
R10	Resistor, MF 10 k 5%, 1/4W	101930
R11	Same as R10	
R12	Resistor, CC 4.7 k 5%, 1/4W	101598
R13	Same as R7	
R14	Same as R9	
R15	Resistor, CC 1.5 k 5%, 1/4W	101577
R16	Resistor, CC 1 k 5%, 1W	101635
R17	Same as R16	
R18	Same as R4	
R19	Same as R5	
R20	Same as R15	
R21	Resistor, CC 100 Ω 5%, 1/4W	101609
R22	Same as R7	
R23	Same as R3	
R24	Resistor, WW 0.1 Ω, 5W	102218
R25	Resistor, CC 100 Ω 5%, 1W	101856
R26	Same as R10	
R27	Same as R10	
R28	Same as R12	
R29	Same as R7	
R30	Same as R9	
R31	Resistor, CC 330 Ω 5%, 1W	101624
R32	Resistor, CC 220 Ω 5%, 1/4W	101566
R33	Same as R32	
R34	Resistor, CC 39 Ω 5%, 1/2W	101733
R35	Same as R34	
U1	Integrated Circuit, 723PC	025761
U2	Same as U1	
U3	Integrated Circuit, 747PC	045205
XF2,3	Socket, Fuse	116299
XQ1,3,4,5,7	SOCKET, Pin	102442
XU1-3	Socket, IC 14-pin	102433
	Socket, Pin (Q2,Q6)	103037
	Test Point, Red +5V	100541
	Test Point, Black Ground	100542
	Test Point, Green -5V	100543
	Test Point, Blue +15V	100547
	Test Point, Vilot -15V	100548

CIRCUIT DESCRIPTION
DISPLAY ASSEMBLY
SCHEMATIC #041945-7-2

1) GENERAL

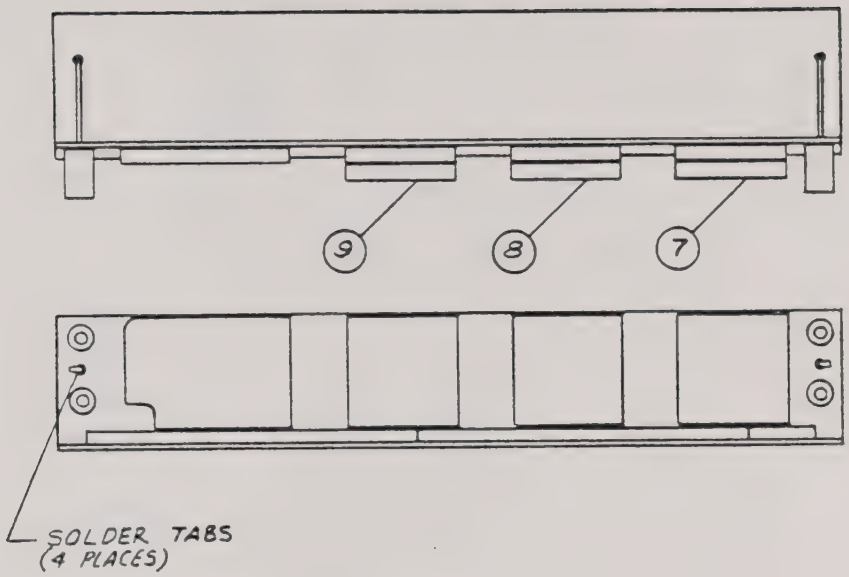
The basis display assembly has three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in hours, minutes and seconds. LED colons are provided between the tubes. The assembly includes provision for the addition of a 3-digit days display plus a third colon when the Days Option is included. Time information is accepted in parallel BCD form. A voltage regulator is used to regulate the approximately +220 V input down to 180 V for use by the display tubes.

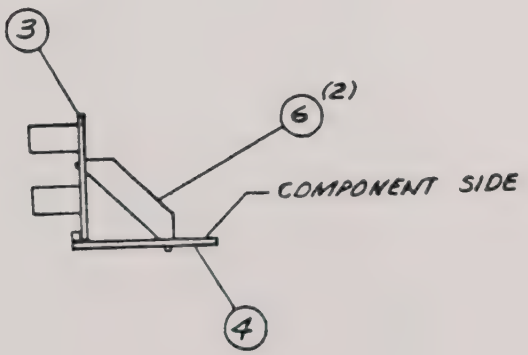


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
2. ALL DIODES ARE FLV-100.
3. ALL IC'S ARE DD-700.

READOUT & DRIVER
SCHEMATIC #041945-7-2 REV G



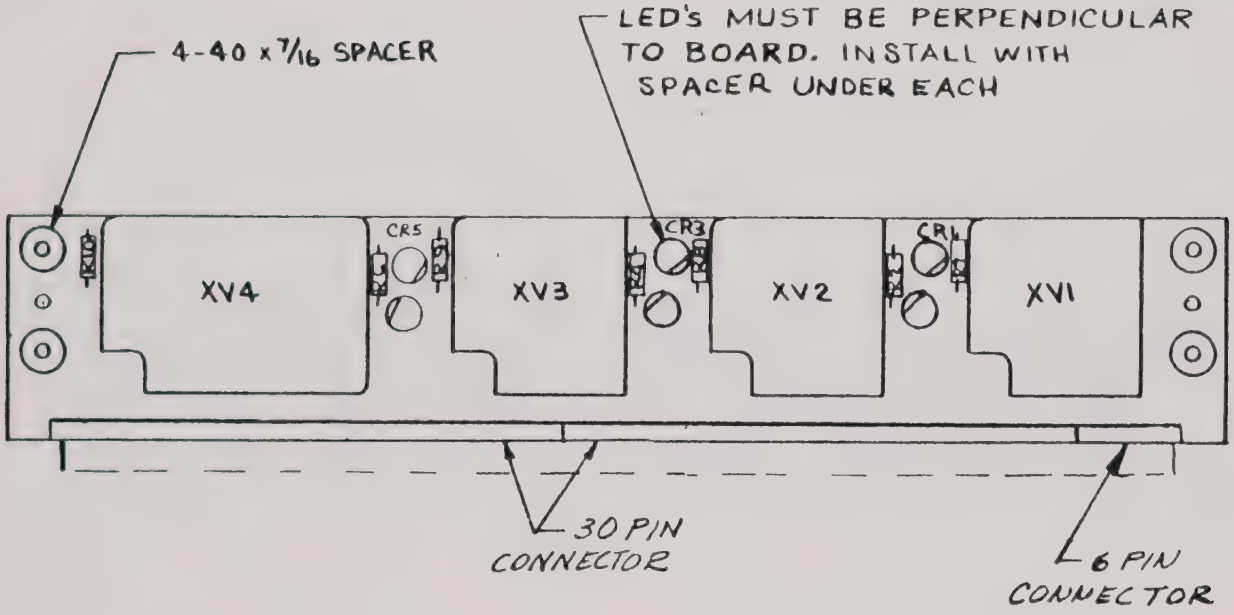


DISPLAY ASSEMBLY, 6-DIGIT #041945-4-2 REV E_1

PARTS LIST

6-DIGIT DISPLAY ASSEMBLY #041945-7-2 REV F

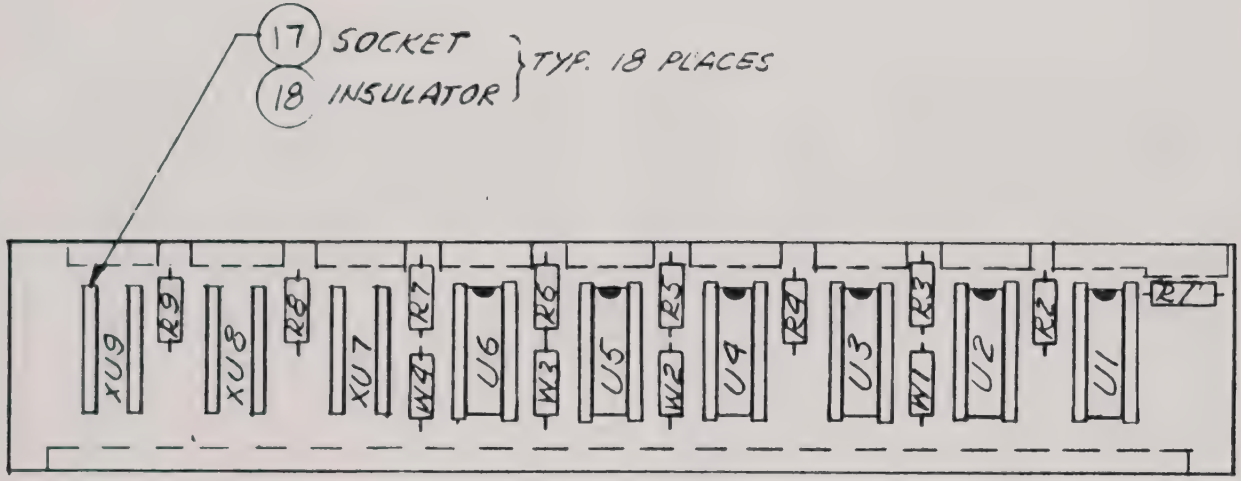
REF.	DESCRIPTION	SD PART NO.
	Assembly, Display and Driver	041945-4-2
	Assembly, Display	041766-4-1
	Assembly, Driver	041772-4-1
	Schematic	041945-7-2
V1-3	Display Tube, SP 352 Sperry	102403
	Bracket, Display and Driver Board	051450



NOTE:
1.) CR 5 & 6 MOUNTED WITH DAYS OPTION ONLY.

DISPLAY BOARD, 9-DIGIT #041766-4-1 REV G_2

8152-7-79



NOTE
1.) DOTTED AREAS TO BE MASKED BEFORE FLOW SOLDERING.

9-DIGIT DISPLAY DRIVER ASSEMBLY #041772-4-1 REV D_1

5-72

PARTS LIST

DISPLAY ASSEMBLY #041766-4-1 REV G

REF.	DESCRIPTION	SD PART NO.
	Assembly	041766-4-1
	Schematic	041945-7-2
CR1-4	Lamp, LED	100455
R1	Not Used	
R2	Resistor, 120 Ω 5%, 1/4 W, CC	101717
R3	Not Used	
R4	Same as R1	
R5	Not Used	
R6	Same as R2	
R7-10	Resistor, 4.7 k 5%, 1/4 W, CC	101598
XV1-3	Socket, Display 2-digit	102445
XV4	Socket, Display 3-digit	102446
	Connector, 30-pin Right Angle Male	101277
	Connector, 6-pin, Right Angle	07189106
	Spacer, Swage, 4-40x. 437 Lg.	101062
	Spacer, LED Lamp	101077

DISPLAY ASSEMBLY #041772-4-1 REV F

REF.	DESCRIPTION	SD PART NO.
	Assembly	041772-4-1
CR7	Diode, 1N5297	100457
Q1	Transistor, 2N3440	101420
R1-9	Resistor, 10 k 5%, 1/4 W	101570
U1-6	Integrated Circuit, TTL	045203
VR1	Diode, 1N991B	100461
W1-4	Jumper, Molded	102879
	Socket, Integrated Circuit 16-pin	103350

CHAPTER 6
STANDARD OPTIONS

6.1 GENERAL

Several standard options are available for the Model 8152. All options, when supplied with the instrument, will be described on the following pages.

CIRCUIT DESCRIPTION
HIGH STABILITY OSCILLATOR (OPTION B11/B13)
SCHEMATIC #7-061163

1) GENERAL

Options B11 and B13 provide a precision, high stability, crystal (3 MHz) oscillator in place of the 1 MHz time base normally used in this unit.

Referring to the schematic, the above options add Oscillator Assembly #071128XX, a rear panel connector, J12, rear panel switch S1 and related components and wiring to the basic unit.

2) SPECIFICATIONS

Time Base:

B13:	Stability:	±4 parts in 10^9 for 20°C change within the range from -20°C to +55°C.
	Aging Rate:	1 part in 10^9 per 24 hours after 72 hours warm-up.
B11:	Stability:	4 parts in 10^9 for 20°C change within 0°C to +55°C.
	Aging Rate:	5 parts in 10^{10} per 24 hours after 72 hours warm-up.

External Time Base:

Accepts a 1 MHz input at 1 V peak-to-peak (nominal) into a 1 kΩ via a rear panel BNC type connector. A rear panel s switch selects INTernal or EXTernal time base. On INTernal, a 1 MHz, 5 V TTL signal is available on the rear BNC connector.

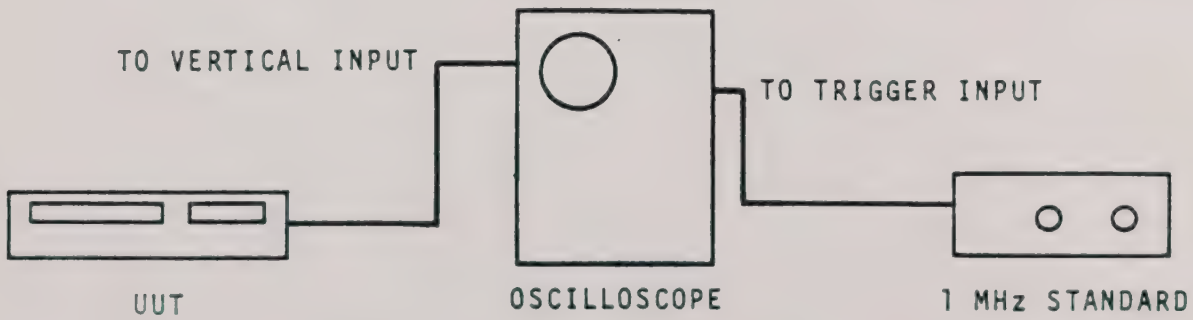


FIGURE 1 OSCILLATOR ACCURACY TEST

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

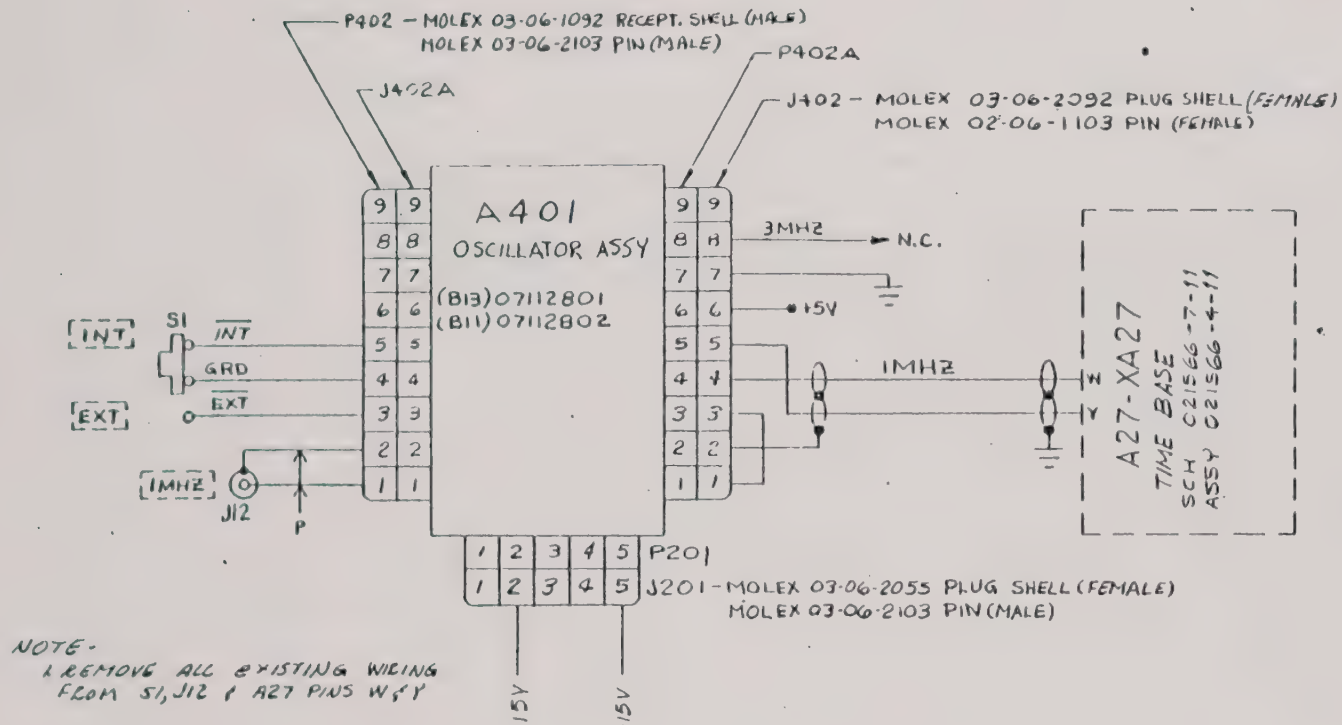
To check oscillator frequency (not stability):

1) Trigger the oscilloscope externally with the 1 MHz standard.
2) Connect a 1 MHz frequency from the Model 8120 1 MHz BNC to the vertical input of the oscilloscope.
3) Set the oscilloscope sweep time to 0.1 μsec/cm and adjust the controls to obtain a presentation of one to two cm vertical deflection.
4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10^7. If necessary, adjust the oscillator (fine frequency Adj, coarse if necessary).

TABLE 1 OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6
1 cm/sec	1 part in 10^7
1 cm/10 sec	1 part in 10^8
1 cm/100 sec	1 part in 10^9

REV	DESCRIPTION	BY	CHK	DATE
A	RELEASED TO RECORDS			7/72



NOTE-
1. REMOVE ALL EXISTING WIRING FROM S1, J12 & A27 PINS W & Y

LIST OF MATERIALS

CONCORD CALIFORNIA

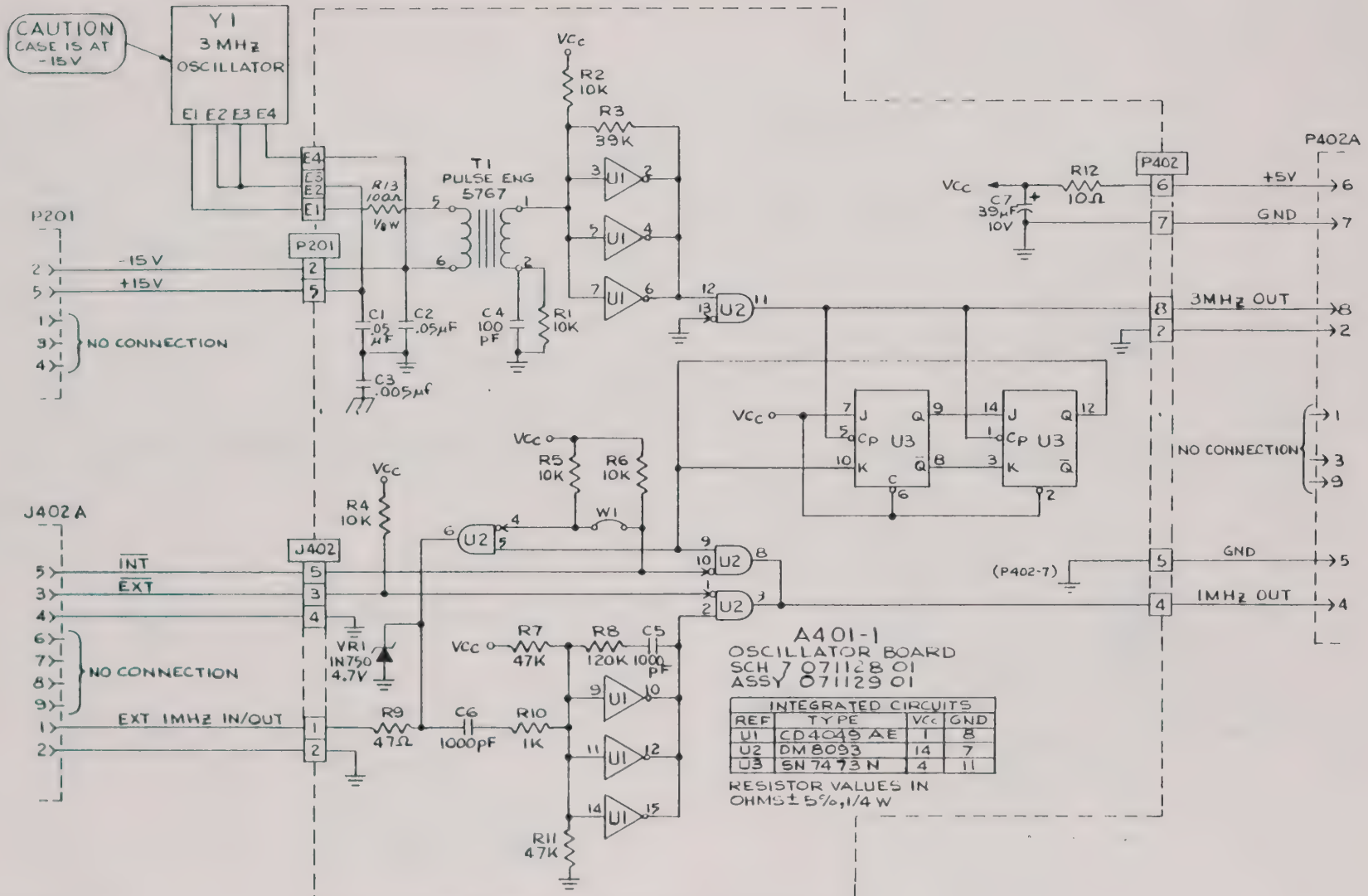
CODE IDENT 51917

811-B13 0
111 STAB 0S

06116327

PARTS LIST
OPTION B11 - HIGH STABILITY OSCILLATOR
#06116328 REV A_1

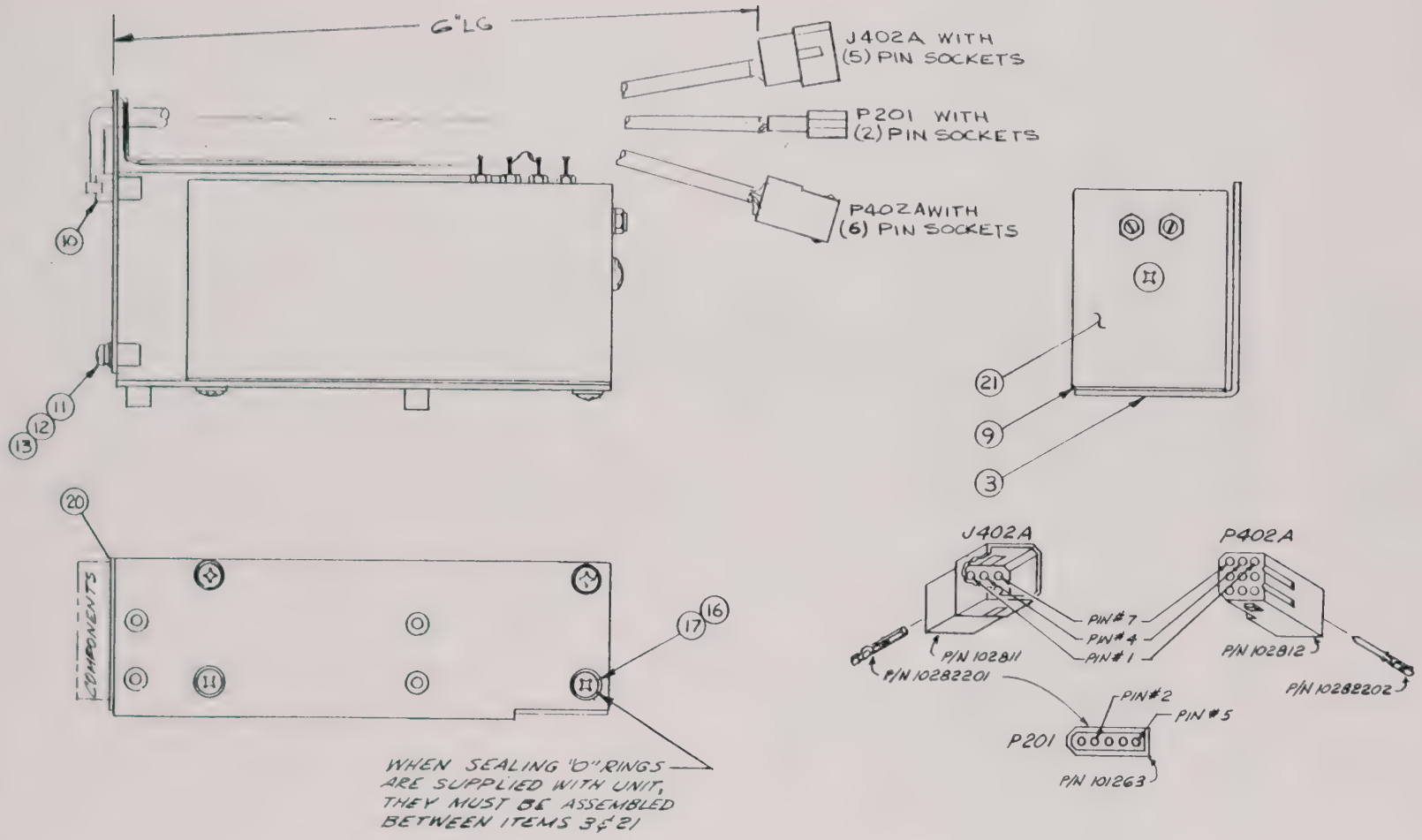
REFERENCE	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-06116327
A401	Assembly, Oscillator	07112801
J402	Plug Shell, 9 Position Contact, Female	102811 10282201
P402	Receptacle Shell, 9 Position Contact, Male	102812 10282202
J201	Receptacle Shell, 5 Position Contact, Female	101264 10282201
	DELETE	
	Oscillator Cover Plate	051913



NOTES:
1. FOR B11, Y1 PER S-D 033429.
FOR B13, Y1 PER S-D 033427.

SCHEMATIC HIGH STABILITY OSCILLATOR #7-07112801 REV D,

07112801



ASSEMBLY HIGH STABILITY OSCILLATOR #07112801 REV A_1

OPTIONS B11/B13-6

CIRCUIT DESCRIPTION
LATCHED BUFFER
SCHEMATIC #7-02168502/16

1) GENERAL

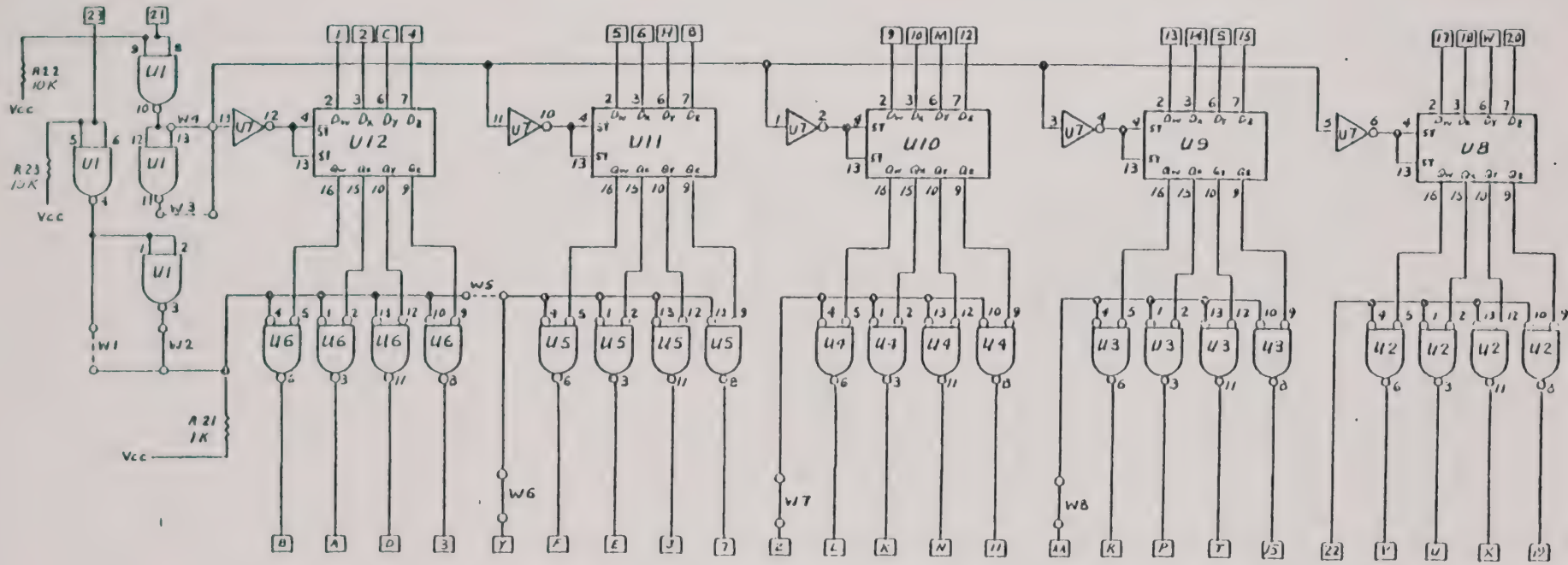
These cards each contain five quad-latches and 20 non-inverting buffers.

2) FUNCTION

Each of the latches (U8-U12) has the property that a signal applied to a "D" input input is transferred to the corresponding "Q" output when the $\overline{ST}$ input is high, i.e. "Q" will copy "D" when $\overline{ST}$ is high. The "Q" output retains its last state when $\overline{ST}$ is low. The $\overline{ST}$ inputs are controlled via pin 21, U1-10 and inverters on U7.

The output buffers on U2-U6 gate the contents of the latches onto the associated output lines. These buffers are controlled in groups of four via pins 23, Y, Z, AA and 22 on the #02168502 Assembly. The #02168516 Assembly differs in that jumper W5 is installed, thus controlling gates on U5 and U6 from pin 23 through drivers on U1. Driver U1-3 output is available at pin Y.

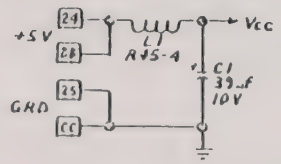
A	SN74LS75N WAS SN7475N			



NOTE: UNLESS OTHERWISE SPECIFIED

1. RESISTORS: 10 KΩ, ¼ W, C.C.

3. I.C. MC8T97P - U1.
   " MC1808P - U2, U3, U4, U5 & U6.
   " SN7404N - U7.
   PIN 7 IS CONNECTED TO GRD.
   PIN 14 " " " Vcc.
4. I.C. SN74LS75N - U8, U9, U10, U11 & U12
   PIN 12 IS CONNECTED TO GRD.
   PIN 5 " " " Vcc.



LATCHED BUFFER

7 02168502 B

PARTS LIST
1 MHZ BUFFERED OUTPUT
#07187603 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-07187603
J18	Connector, BNC	101155
	Insulator, BNC	100823
	Fiber Washer	101074
J4	Cover Plate	021398-1-2
	DELETE	
J4	Cover Plate	021398-1-1

2. 2. Set the DAYS/ID digits.

3. Set the mode switch to GEN.

4. At some time before the start pulse will occur, position the START switch to AUTO and hold it there until after the start pulse has occurred.

The TCG is now synchronized to within µs of the start pulse.

The TCG may be started manually at any time by positioning the mode switch to GEN and then momentarily positioning the START to MAN. The time-of-day and DAYS/ID registers may first be preset if desired while the mode switch is in STOP.

NOTE

When this option is used with 8150's equipped for XR3 codes, two out of the six Adv./Ret. rates are not as indicated on the front panel silkscreen. The 10 µS/S rate is actually 5 µS/S and the 100 µS/S rate is actually 25 µS/S.

CIRCUIT DESCRIPTION
EXTERNAL/WWV SYNCHRONIZATION (Option S11A)
SCHEMATIC #7-051875

1) GENERAL

This option provides two basic starting capabilities:

a) External Synchronization

The clock or generator is automatically started in synchronism with an external pulse. Starting accuracy to within 1 µs can be expected exclusive of start pulse rise time delay. Controls are included for advancing or retarding the time base at precise rates to allow resynchronization without interruption of time accumulation.

b) WWV Synchronization

Allows full synchronization of the clock or generator to radio stations WWV in Fort Collins, Colorado or WWVH in Puunene, Maui, Hawaii. Controls and included to correct for transmission advance/retard the time base for resynchronization.

Changes to the basic unit are shown on the attached Schematic. The following connectors and controls are added:

1) A rear panel BNC connector to accept the external start command.
2) A rear panel BNC connector to accept the WWV input.
3) A front panel BNC connector to allow access to the TICK and PEDestal (or internal 1 pps) output.
4) A front panel AUTO/MANual START control switch.
5) Front panel controls to select the advance/retard rate and direction.
6) Front panel thumbwheel switches to correct for transmission propagation delays.
7) Front panel TICK and ON TIME indicators.

2) SPECIFICATIONS

EXTERNAL START PULSE: A positive going level change of +4.5 V, minimum, for duration of not less than 5 µs. Input impedance in 10 kΩ. Up to 50 V may be applied without damage.

WWV SYNC INPUT: Unit will detect the WWV (1 kHz) or WWVH (1.2 kHz) second ticks with a minimum input level of 0.5 Vrms.

ADVANCE/RETARD RATES: 1 usec/sec., 10 usec/sec., 100 usec/sec., 1 msec/sec., 10 msec/sec., 100 msec/sec.

PROPAGATION DELAY: Three thumbwheel swithes allow inserting a compensation for propagation delays of up to 99.9 ms in 0.1 msec. increments.

3) EXTERNAL START OPERATING INSTRUCTIONS

A pulse (see specifications) is applied to the EXT START input on the rear panel.

NOTE

The TICK and ON TIME lamps are not used in the EXT Start Mode.

1) The propagation delay switches may be used if applicable; if not, set them to 00.0 ms.

2) Position the Mode switch to STOP for 1 second, minimum.

METHOD #1

a) Position the Mode switch to HOLD.
b) Position the START switch to AUTO and hold it until the next pulse occurs.
c) Preset desired start time as described elsewhere in this manual.

METHOD #2

a) Preset the desired start time.
b) Set the Mode switch to GEN or RUN.
c) At some time before the start pulse will occur, position the START switch to AUTO and hold it there until after the start pulse has occurred.

The unit is now synchronized to within 1 µs of the start pulse. The instrument may be started manually at any time by positioning the Mode switch to GEN or RUN and then momentarily positioning the START switch to MAN. The unit may first be preset if desired while the Mode switch is in STOP.

4) WWV SYNC OPERATING INSTRUCTIONS

EQUIPMENT REQUIRED:

1) WWV Receiver: Tick Output; 0.5 Vrms, minimum.
2) Oscilloscope: Vert: 0.5 V/div, 100 kHz bandwidth, minimum.
Horiz: 0.5 to 5 mS/div. (Oscilloscope required only when precision must be better than +3 mS.)

SETUP:

1) Connect the Tick Output of the receiver to the "WWV IN" BNC on the rear of the Time Code Generator (TCG).

2) Adjust the Tick Output of the receiver for about 3 V p-p (1.5 V p-p minimum). This will correspond to about 1 V p-p on the TICK and PED BNC.

START-UP:

1) Note that the TICK lamp is flashing one each second.

2) Set the 3 PROPAGATION DELAY switches (XX.X ms) to the calculated time required for the signal to propagate from the transmitter to the receiver.

3) Place the Mode switch in HOLD position.

4) Momentarily position the START switch to MANUAL.

5) Place the Mode switch in the STOP position for a minimum of 1 second.

6) Position the Mode switch to HOLD.

7) Make certain that a good clean tick signal is present; then position the START switch to AUTO and hold for 1 second.

8) The unit is now synchronized to within +10 mS*. Synchronization using an ON TIME lamp or scope may be performed for greater accuracy.

SYNCHRONIZATION USING ON TIME LAMP:

1) Position the PER SEC switch to 1 mS.
2) Hold the ADV/RET switch in the RET position until the ON TIME lamp stops flashing.
3) Hold the ADV/RET switch in the ADV position until the ON TIME lamp flashes and then stops flashing; note haw many flashes this requires.
4) Hold the ADV/RET switch in the RET position for 1/2 the number of flashes counted in this position less 2.
5) Synchronization is now accurate to within +2 mS*.

SYNCHRONIZATION USING A SCOPE:

1) Connect the vertical input of the scope (0.5/div and 2 mS/div) to the TICK and PED BNC on the front panel of the unit.
2) Observe the pedestal and tick on a common baseline.
3) Select a convenient rate on the PER SEC switch and, using the ADV/RET switch, superimpose the tick and pedestal as shown in Figure 1.
4) Return the PER SEC switch to OFF.
5) Synchronization is now accurate to within +100 mS*.

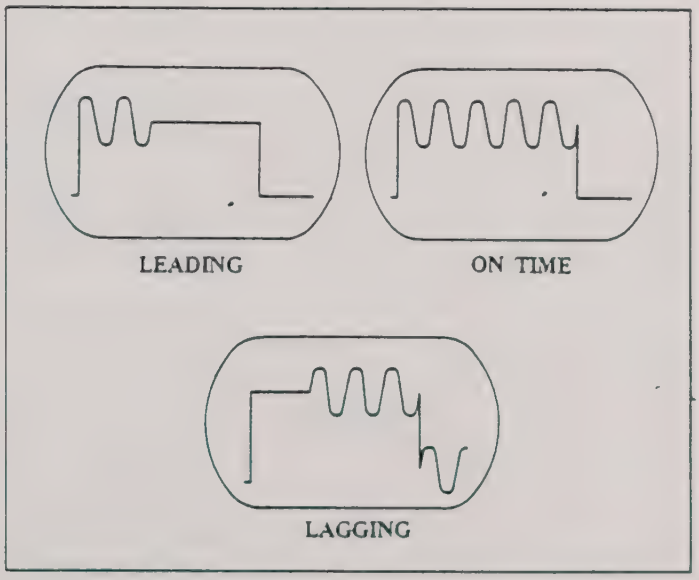


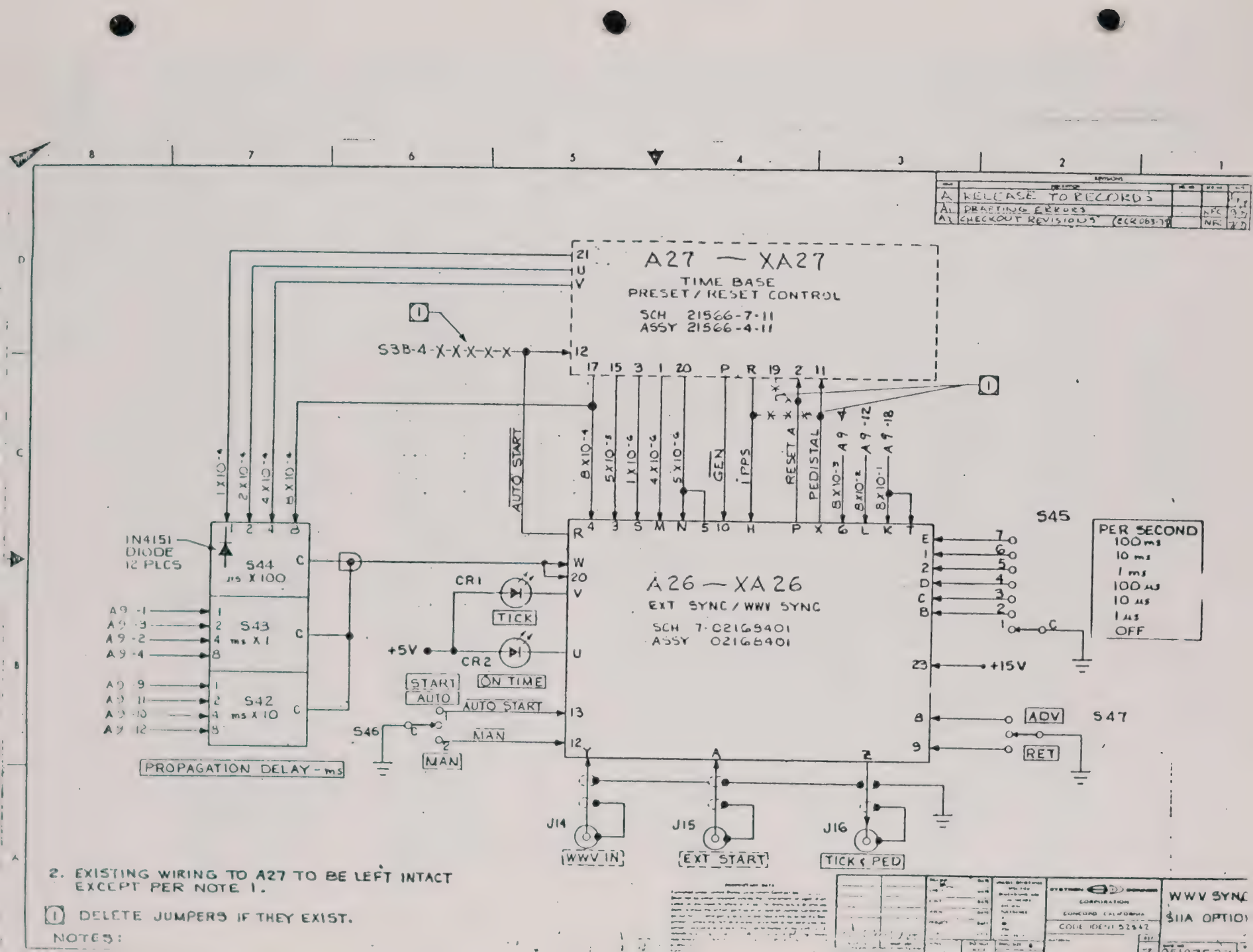
FIGURE 1 TICK AND PEDESTAL

* Any uncertainity in the propagation delay time must be added to these figures.

PARTS LIST
WWV SYNCHRONIZATION (OPTION S11A)
#05187537

REFERENCE	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-05187537
A26	Assembly, Ext. Sync	2168401
	Trim Insert	051162-1-1
	Nomen Panel	06117207
CR1	LED HP5082-4440	100456
CR2	Same as CR1	
S42	Switch Assembly, Thumbwheel	05130011
S43	Same as S42	
S44	Switch Marking	051374
S45	Switch Assembly, Rotary	06134406
S46	Switch, Toggle	102336
S47	Switch, Toggle	102323
	Switch Thumbwheel Mounting Bracket	102359
	Switch, Thumbwheel Mounting Strap	10236703
	Switch Knob	102954
	Switch Dress Nut	100893
J14	Connector, BNC	101155
J15	Same as J14	
J16	Connector, BNC	101170
	Insulator BNC	100823
	Fiber Washer	101074
	Solder Lug BNC	100495
	Card Guide	021340-1-2
XA26	Connector, 50-Contact	101204
	DELETE	
	Trim Insert	041774-1-1
	Nomen Panel	051936
J14	Hole Plug BNC	100952
J15	Same as J14	

A	RELEASE TO RECORDS			
A1	DRAFTING ERRORS		APC	
A2	CHECKOUT REVISIONS (ECR 083-79)		NR	



2. EXISTING WIRING TO A27 TO BE LEFT INTACT EXCEPT PER NOTE 1.

[1] DELETE JUMPERS IF THEY EXIST.

NOTES:

WWV SYNC
$11A OPTION

CIRCUIT DESCRIPTION
WWV SYNC/AUTO START
SCHEMATIC #7-021684

1) GENERAL

This card provides control of the advance/retard system, extracts the "tick" from a WWV signal, generates a delayed pedestal, controls the auto start flip-flop on the time base board and provides control for tick and on-time lights.

2) ADVANCE/RETARD CIRCUIT

The advance/retard circuit allows "adding" or "subtracting" timebase counts at a selectable rate. Any one of 6 rates may be selected by grounding the appropriate control line. For example, grounding the 100 µs/s line will put a high on U8-8 pin 10 via inverter U1-12. This allows the 8×10^{-3} rate to set flip-flop U10-3, U4-12. (A negative going transition is produced by differentiating network C2,R10,R11 one hundred times per second setting the flip-flop each time.)

To cause the accumulated count to advance, the first decade divider on the time base board must be reset to zero early; that is at a count of 9 instead of 0. (The usual carry to the next decade is produced.) To retard, the decade is reset to 0 at a count of 1. This causes the decade to lose a count. (No carry is produced.)

Gates U4-6 and U4-8 are used to determine the proper reset point. If advance is selected by grounding the $\overline{\text{ADV}}$ line, gate U9-8 output will go high allowing the output of U4-6 to go low when the 4×10^{-6} and $.5 \times 10^{-6}$ lines are high, (count of 9 from the first decade on the time base board). This low signal will cause flip-flop U10-3, U4-12 to reset producing a negative going transition via differentiator C3, R12,R13. This signal is inverted by gate U10-11 and used to reset the first time base decade. Similarly, if the $\overline{\text{RET}}$ line is grounded, the reset pulse will occur at a count of 1. The rate being used to reset flip-flop U10-3,U4-12 determines the number of times per second the reset pulse is produced.

3) AUTO START

This circuit permits use of an external start signal. Provision is also made to accept the output of the WWV Sync circuit, when used, as a start signal.

The external start signal, on pin A, is differentiated by C4,R17 then inverted by Q1. (A positive going transition of 4.5 V minimum for 5 µs minimum is required on pin A.) Gate U5-8 inverts the output of Q1. (The signal from the WWV circuit also inputs U5-8.) When the AUTO START line is grounded (via a front panel switch) U2-2 output goes high, enabling U3-3. The first time U5-8 goes high, the start flip-flop on the time base card will be set by the signal at pin R provided the unit is in GEN (RUN) or HOLD.

4) WWV SYNC CIRCUIT

The audio signal from a WWV receiver is fed into a circuit which amplifiers the 5 cycles of 1 kHz which comprise the 1 second "TICK" and rejects everything else. The operation of the filter (Q4,Q5,Q6) is as follows; the input signal is applied to the base of Q4, a constant current generator. Q1 is an amplifier with C11 providing ca capacitor feedback. This makes the output of the amplifier appear like an inductive reactance. Capacitor C8 gives the circuit the electrical properties of a tuned circuit. The output from this filter, through source follower Q5 is further processed by the diode/RC network on the base of Q3. When sufficient amplitude has built up

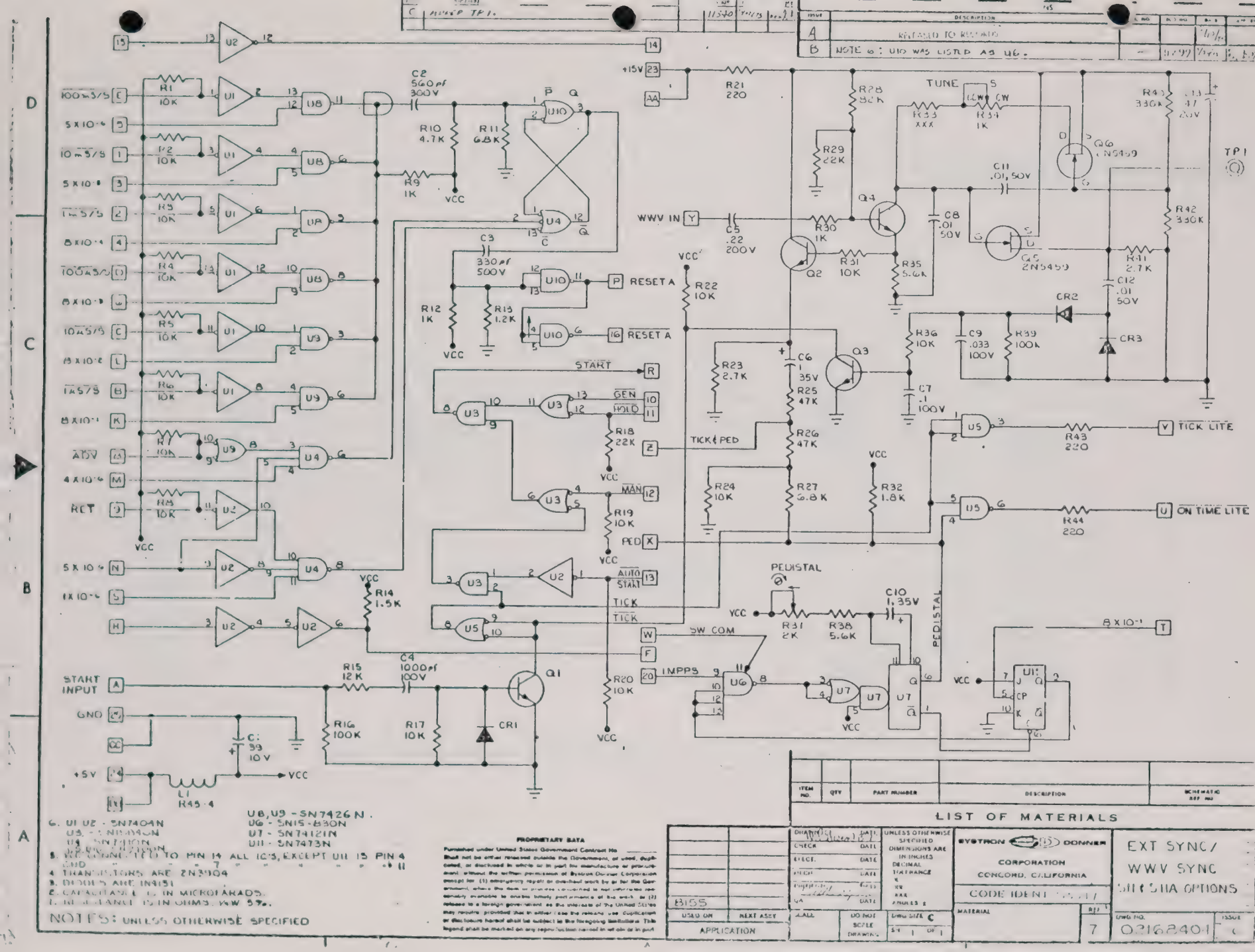
(in about 2 cycles) Q3 conducts producing a negative going pulse which feeds the AUTO START circuit via gate U5-8. Q2 is used to feed the tick signal to the resistive summer which produces the tick and pedestal output.

5) PEDESTAL GENERATOR

The pedestal is a positive pulse of 5 ms duration whose leading edge is delayed from the 1 pps signal by the time set on the propagation delay switches. These switches form a comparator. The output commons are wired through pin W to the expander input to gate U6-8. This line goes positive at coincidence between the switch settings and the parallel, BCD (0.1 ms through 10 ms) inputs to the switches. The other 2 inputs to U6-8 are a 1 pps (or 1 pp frame) signal from flip-flop U11 and a 1 Mpps strobe from the time base card. Flip-flop U11 is set on the leading edge of the 1 pps (or 1 ppF) signal through pin T. When the propagation delay switches reach coincidence U6-8 output goes low firing one-shot U7. U7-6 output is the pedistal signal. U7-1 output resets U11.

6) LED DRIVERS

U5-3 provides a current sink for an LED which indicates the presence of a tick. The tick signal comes from Q3 through U5-8. (Note that an external start signal will also light the LED.) U5-6 is the driver for the on-time LED. U5-6 output will be low when the tick and pedestal signals occur simultaneously, lighting the LED.



REV	DESCRIPTION	BY	DATE
A	RELEASED TO RECORDS		11/7/69
B	NOTE 6: U10 WAS LISTED AS U6.		3/7/70

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE IN OHMS, 1/4W 5%.
2. CAPACITANCE IN MICROFARADS.
3. DIODES ARE IN4151
4. TRANSISTORS ARE 2N3904
5. WIRE CONNECTED TO PIN 14 ALL IC'S, EXCEPT U11 IS PIN 4 GND " " 7 " " " " 11
6. U1 U2 - SN7404N
   U3 - SN5409N
   U4 - SN7420N
   U5 - SN7408N
   U6 - SN5473N
   U7 - SN7473N
   U8,U9 - SN7426N.
   U10 - SN5473N
   U11 - SN7473N

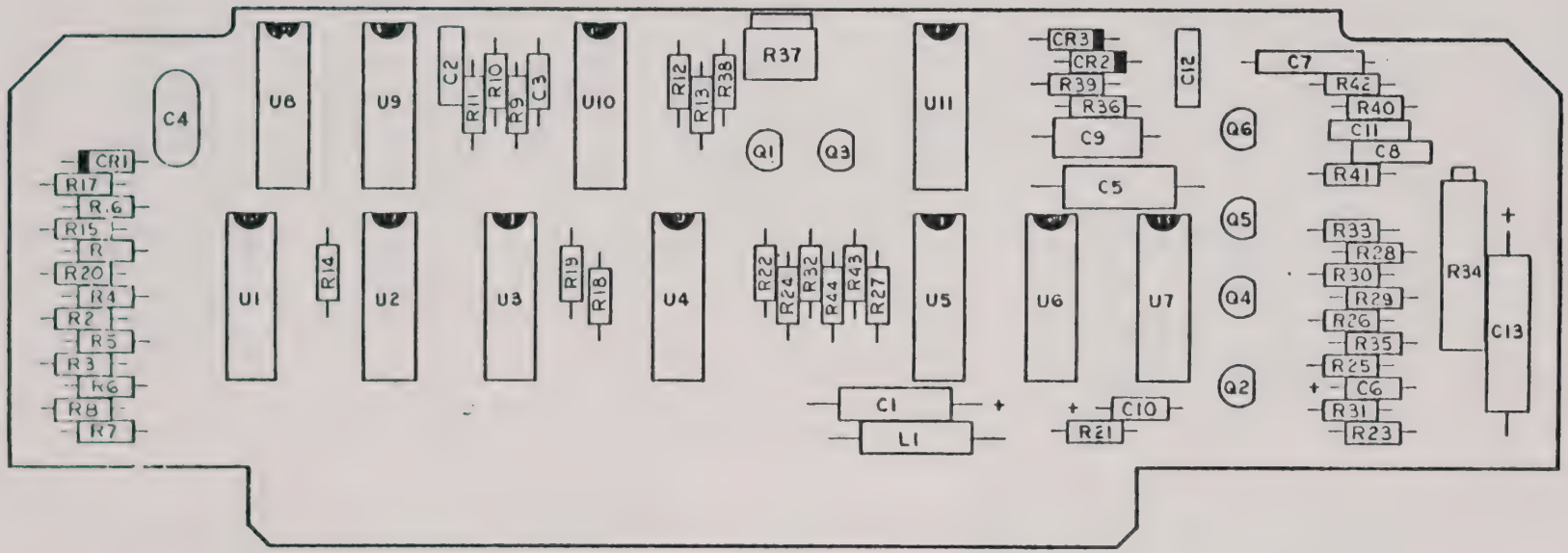
PROPRIETARY DATA

Furnished under United States Government Contract No. _____
Shall not be either released outside the Government, or used, duplicated, or disclosed in whole or in part for manufacture or procurement, without the written permission of Bystron Donner Corporation except for (1) emergency repair or overhaul work by or for the Government, where the item or drawings concerned is not otherwise reasonably available to enable timely performance of the work, or (2) release to a foreign government as the interests of the United States may require, provided that in either case the release use duplication or disclosure hereof shall be subject to the foregoing limitations. This legend shall be marked on any reproduction hereof in whole or in part.

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.01 .XX ±.005 ANGLES ±	BYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	EXT SYNC/ WWV SYNC SHEET 3 OF 3 OPTIONS
CHECK	DATE			
ENGR.	DATE		CODE IDENT	
PROD.	DATE		MATERIAL	REV 7
QA	DATE			DWG NO. 02162401 ISSUE C
B155	NEXT ASSY	DO NOT SCALE DRAWING	DWG SIZE C	SHT 1 OF 1
USED ON				
APPLICATION				


C4
U8
U9
C2
R11
R10
R9
C3
U10
R12
R13
R38
R37
U11
CR3
CR2
R39
R36
C9
C5
C12
C7
R42
R40
C11
C8
R41
Q6
Q5
Q4
Q2
Q1
Q3
CR1
R17
R.6
R15
R
R20
R4
R2
R5
R3
R6
R8
R7
U1
R14
U2
U3
R19
R18
U4
R22
R24
R32
R44
R43
R27
U5
U6
U7
C1
L1
C10
R21
R33
R28
R30
R29
R26
R35
R25
C6
R31
R23
R34
C13

| | | |

PARTS LIST
EXT SYNC/WWV SYNC #02168404 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Dwg. 02168401)	02168404
	Schematic	02168404
C1	Capacitor, 39 µF, 10 V, Tant	100183
C2	Capacitor, 560 pF, 300 V, Mica	100222
C3	Capacitor, 330 pF, 500 V, Mica	100276
C4	Capacitor, 1000 pF, 100 V, Mica	100243
C5	Capacitor, .22 µF, 200 V, Metmyl	100106
C6,10	Capacitor, 1 µF, 35 V, Tant	100082
C7	Capacitor, .1 µF, 100 V, Metmyl	100141
C8,11,12	Capacitor, .01 µF, 50 V, Mylar	100132
C9	Capacitor, .033 µF, 100 V, Metmyl	100142
C13	Capacitor, 47 µF, 20 V, Tant	100186
CR1-3	Diode, 1N4151	100385
L1	Inductor, L45-4	101313
Q1-4	Transistor, 2N3904	101377
Q5,6	Transistor, 2N5459	101384
R1-8,17,19,20,22, 24,31,36	Resistor, 10 k 5%, ¼ W	101570
R9,12,30	Resistor, 1 k 5%, ¼ W	101569
R10	Resistor, 4.7 k 5%, ¼ W	101598
R11,27	Resistor, 6.8 k 5%, ¼ W	101544
R13	Resistor, 1.2 k 5%, ¼ W	101581
R14	Resistor, 1.5 k 5%, ¼ W	101577
R15	Resistor, 12 k 5%, ¼ W	101565
R16,39	Resistor, 100 k 5%, ¼ W	101558
R18,29	Resistor, 22 k 5%, ¼ W	101572
R21,43,44	Resistor, 220 k 5%, ¼ W	101566
R23,41	Resistor, 2.7 k 5%, ¼ W	101599
R25,26	Resistor, 47 k 5%, ¼ W	101574
R28	Resistor, 82 k 5%, ¼ W	101578
R32	Resistor, 1.8 k 5%, ¼ W	101602
R33	Resistor, 0 Ω Nom. 5%, ¼ W	Factory Select
R34	Resistor, 1 k Var., 3/8 W	101680
R35,38	Resistor, 5.6 k 5%, ¼ W	101584
R37	Resistor, 2 k 20%, ½ W, Var.	102105
R40,42	Resistor, 330 k 5%, ¼ W	101658
U1,2	Integrated Circuit, SN7404N	025779
U3	Integrated Circuit, SN15846N	019705
U4	Integrated Circuit, SN7410N	019706
U5,10	Integrated Circuit, SN7400N	--
U6	Integrated Circuit, SN15-830N	019712

PARTS LIST
EXT SYNC/WWV SYNC #02168404 REV A_1 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
U7	Integrated Circuit, SN74121N	025760
U8,9	Integrated Circuit, SN7426N	045252
U11	Integrated Circuit, SN7473N	019709

CHAPTER 7
SPECIAL MODIFICATIONS

7.1 GENERAL

Modifications to the Model 8155, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

CIRCUIT DESCRIPTION
TIME ON DEMAND TO IEEE 488 BUS (DAYS TO SECONDS)
BLOCK DIAGRAM #7-07160210 REV A

1. GENERAL

TALK ONLY ?!

This option provides time on demand to the IEEE 488 Bus in ASCII characters. Time data in days through seconds are presented, most significant digit first, with colons between days and hours, hours and minutes, and minutes and seconds. Carriage return and line feed characters terminate the group.

STRING → DDD:hh:mm:ss<CR><LF>

2. CIRCUIT DESCRIPTION

Referring to the Block Diagram, IEEE Bus Control Cards A1 and A2 provide the basic IEEE Bus Interface via J19. Device Address switches S40 are located on the rear panel. Parallel time data from the Accumulator are loaded into latches on Cards A6 and A7 which are normally in the follow mode. When time is demanded by designating the unit a talker, the time in the latches is frozen and output on the bus under the control of Cards A1 and A2 plus circuits on Time Output Formatter A5. The Controller on the Bus has access to time information at all times provided power to the unit is on.

3. OPERATION

The Interface, as used in this application, will obey the following Bus Commands:

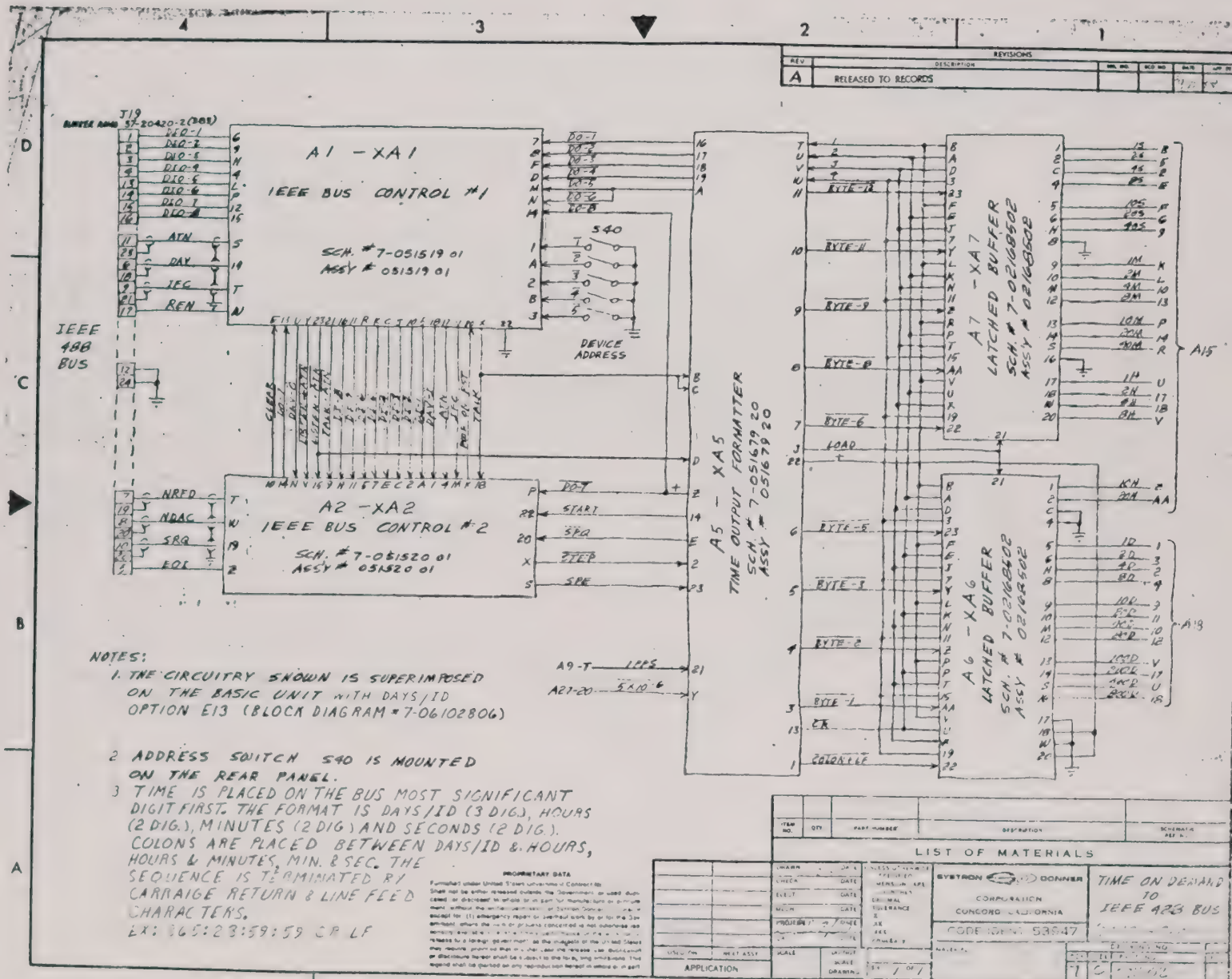
1. IFC - Interface Clear
2. MLA - My Listen Address
3. MTA - My Talk Address
4. UNL - Unlisten
5. UNT - Untalk

PARTS LIST

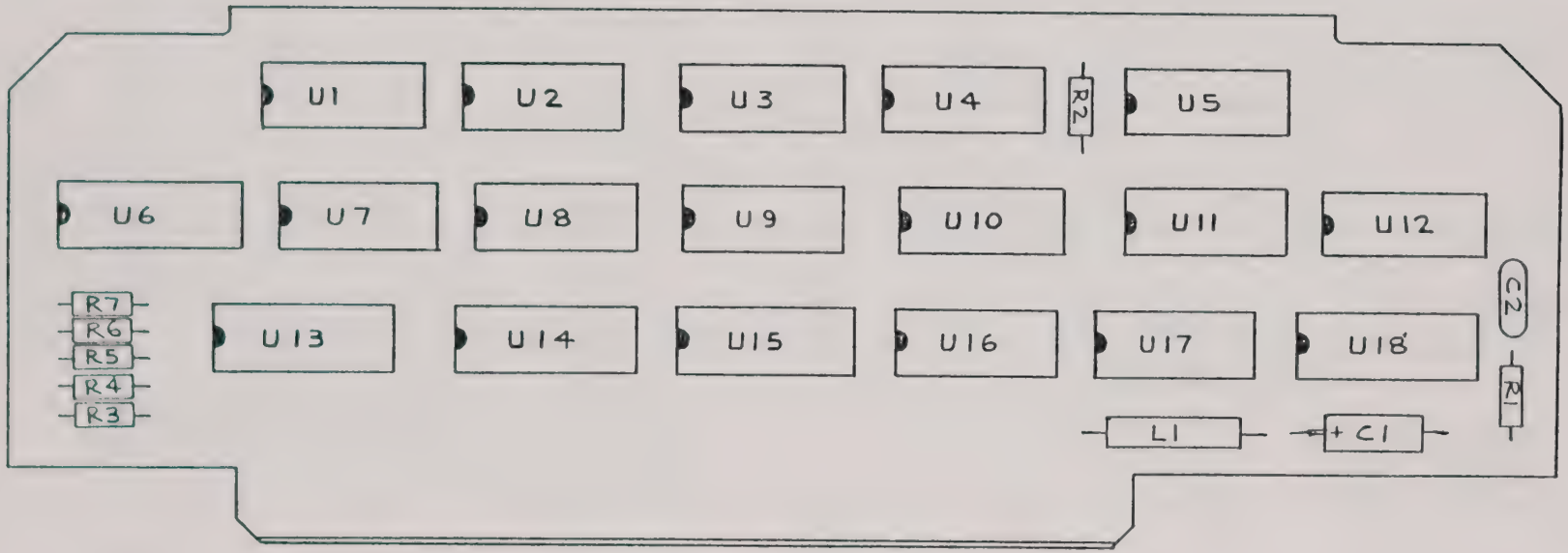
TIME ON DEMAND TO IEEE 488 BUS (DAYS TO SECONDS)

#07160210 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-07160210
A1	Assembly, IEEE BUS Control #1	05151901
A2	Assembly, IEEE BUS Control #2	05152001
A5	Assembly, Time Output Format	05167920
A6-7	Assembly, Latched Buffer	02168502
	Card Guide	021340-1-2
XA1-2,5-7	Connector, 50 Contact	101204
	Rear Panel	05120206
J19	Connector, 24 Contact (57-20420-2)	117054
XS40	Socket (Augat 314-AG6A-3R)	
	Spacer (#2 .437 L x .125 O.D.)	116235
	DELETE	
	Rea	
	Rear Panel	041815-1-2


REVISIONS
REV
DESCRIPTION
A
RELEASED TO RECORDS
A1 - XA1
IEEE BUS CONTROL #1
SCH. # 7-051519 01
ASSY # 051519 01
S40
DEVICE ADDRESS
IEEE 488 BUS
A2 - XA2
IEEE BUS CONTROL #2
SCH. # 7-051520 01
ASSY # 051520 01
A5 - XA5
TIME OUTPUT FORMATTER
SCH. # 7-051679 20
ASSY # 051679 20
A7 - XA7
LATCHED BUFFER
SCH. # 7-02168502
ASSY # 02168502
A6 - XA6
LATCHED BUFFER
SCH. # 7-02168602
ASSY # 02168502
A15
A18
A9-T 1PPS
A21-20 5X10-6
NOTES:
1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON THE BASIC UNIT WITH DAYS/ID OPTION E13 (BLOCK DIAGRAM # 7-06102806)
2 ADDRESS SWITCH S40 IS MOUNTED ON THE REAR PANEL.
3 TIME IS PLACED ON THE BUS MOST SIGNIFICANT DIGIT FIRST. THE FORMAT IS DAYS/ID (3 DIG.), HOURS (2 DIG.), MINUTES (2 DIG.) AND SECONDS (2 DIG.). COLONS ARE PLACED BETWEEN DAYS/ID & HOURS, HOURS & MINUTES, MIN. & SEC. THE SEQUENCE IS TERMINATED BY CARRAIGE RETURN & LINE FEED CHARACTERS.
EX: 065:23:59:59 CR LF
LIST OF MATERIALS
SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
TIME ON DEMAND TO IEEE 488 BUS
APPLICATION

REVISIONS				
REV	DESCRIPTION	PC NO	ECO NO	DATE
A	RELEASED TO RECORDS			
B	SHT 2 REDRAWN (NEW A/N).	—	11403	



LIST OF MATERIALS

CONCORD CALIFORNIA

CODE IDENT 53947

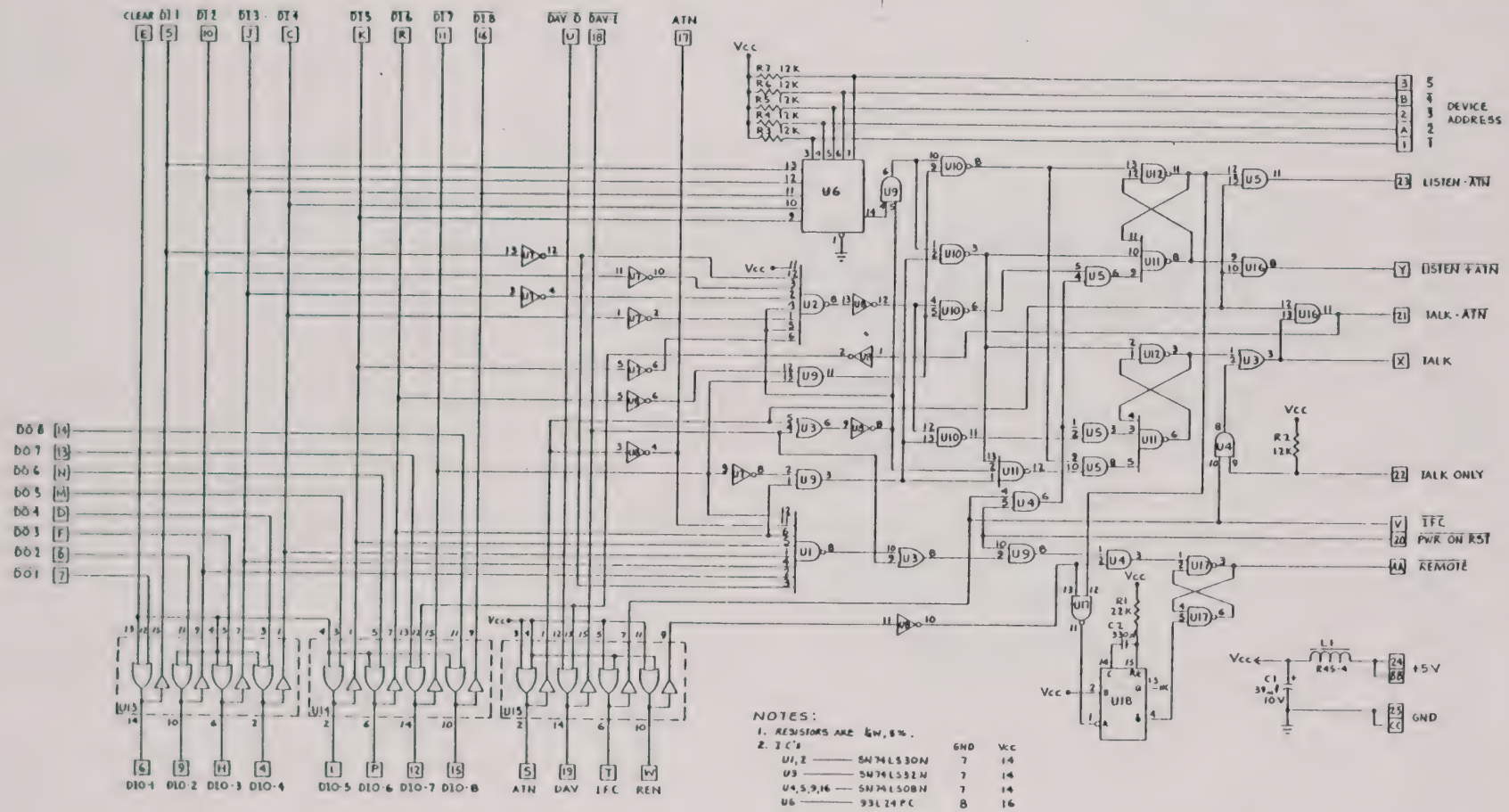
P.C.BDA
IEEE BU
CONTROL

9155-04724
9131-04711

APPLICATION

2/1

1051519



NOTES:

1. RESISTORS ARE ¼W, 5%.
2. I C's

		GND	Vcc
U1, 2	SN74LS30N	7	14
U3	SN74LS32N	7	14
U4, 5, 9, 16	SN74LS08N	7	14
U6	93L24PC	8	16
U7, 8	SN74LS04N	7	14
U10, 12, 17	SN74LS00N	7	14
U11	SN74LS10N	7	14
U13, 14, 15	MC3446P	8	16
U18	SN74LS123N	8	16

LIST OF MATERIALS

SCHEMATIC, IEEE BUS CONTROL #1

COOP IDENT 53947

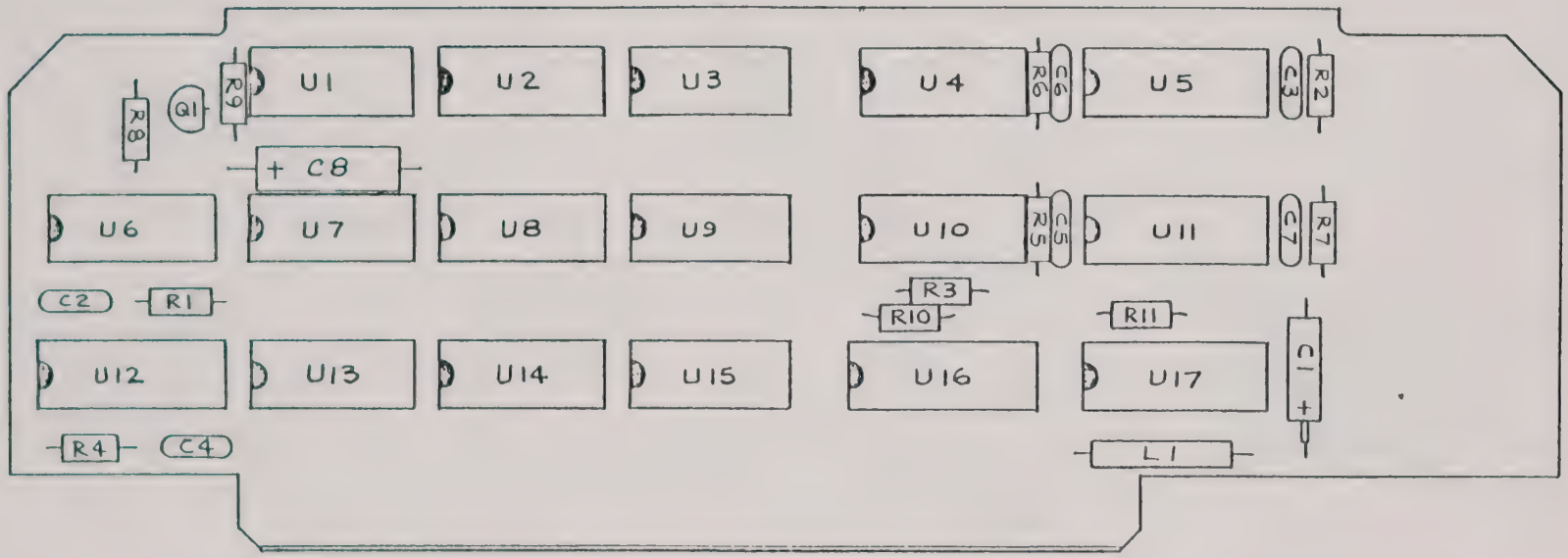
7 D 05/15/1901 B

PARTS LIST

P.C. BOARD ASSEMBLY, IEEE BUS CONTROL #1 #05151901 REV A

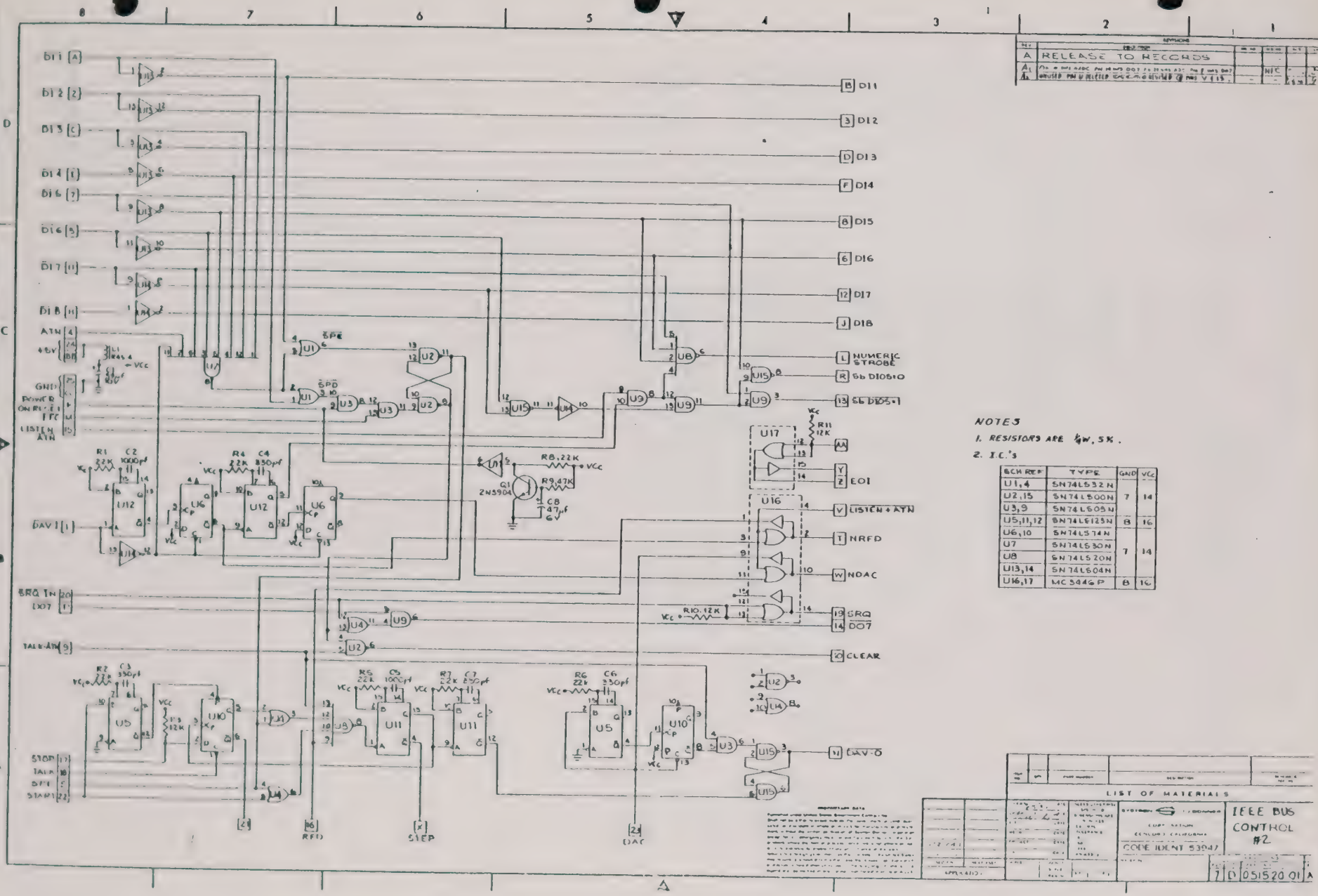
REF.	DESCRIPTION	SD PART NO.
	Assembly	05151901
	Schematic	7-05151901
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 330 pF, DM	100276
L1	Inductor, R45-4	101313
R1	Resistor, 22 k, ¼ W	101572
R2-7	Resistor, 12 k, ¼ W	101565
U1,2	Integrated Circuit, SN74LS30N	103971
U3	Integrated Circuit, SN74LS32N	103972
U4,5,9,16	Integrated Circuit, SN74LS08N	103967
U6	Integrated Circuit, 93L24PC	117020
U7,8	Integrated Circuit, SN74LS04N	103749
U10,12,17	Integrated Circuit, SN74LS00N	103130
U11	Integrated Circuit, SN74LS10N	103968
U13,15	Integrated Circuit, MC3446	117021
U18	Integrated Circuit, SN74LS123N	103976
	Extractor	100865

REVISIONS				
A	RELEASED TO RECORDS			
A1	CORRECTED C8 ORIENTATION		WFC	



LIST OF MATERIALS

BYSTRON DYNAMICS CORPORATION CONCORD CALIFORNIA	P.C. BD. ASSY. IEEE BUS CONTROL II
CODE IDENT 63947	05152001



NOTES

1. RESISTORS ARE ¼W, 5%.
2. I.C.'s

SCH REF	TYPE	GND	VCC
U1,4	SN74LS32N	7	14
U2,15	SN74LS00N		
U3,9	SN74LS05N		
U5,11,12	SN74LS125N	8	16
U6,10	SN74LS74N	7	14
U7	SN74LS30N		
U8	SN74LS20N		
U13,14	SN74LS04N		
U16,17	MC3446P	8	16

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE TO RECORDS		
A1		NFC	

LIST OF MATERIALS

IEEE BUS CONTROL #2

CODE IDENT 53947

051520 01 A

PARTS LIST

P.C. BOARD ASSEMBLY, IEEE BUS CONTROL #2 #05152001 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly	05152001
	Schematic	7-05152001
C1	Capacitor, 39 μF, 10 V	100183
C2,5	Capacitor, 1000 pF, D.M.	100243
C3,4,6,7	Capacitor, 330 pF, D.M.	100276
C8	Capacitor, 47 F, TANT	100224
L1	Inductor, R45-4	101313
Q1	Transistor, 2N3904	101377
R1,2,4-8	Resistor, 22 k, ¼ W	101572
R3,10,11	Resistor, 12 k, ¼ W	101565
R9	Resistor, 47 k, ¼ W	101574
U1,4	Integrated Circuit, SN74LS32N	103972
U2,15	Integrated Circuit, SN74LS00N	103130
U3,9	Integrated Circuit, SN74LS08N	103967
U5,11,12	Integrated Circuit, SN74LS123N	103976
U6,10	Integrated Circuit, SN74LS74N	103132
U7	Integrated Circuit, SN74LS30N	103971
U8	Integrated Circuit, SN74LS20N	103969
U13,14	Integrated Circuit, SN74LS04N	103749
U16,17	Integrated Circuit, MC3446	117021
	Extractor	100865

CIRCUIT DESCRIPTION
TIME OUTPUT FORMATTER
SCHEMATIC #7-05167920

1) GENERAL

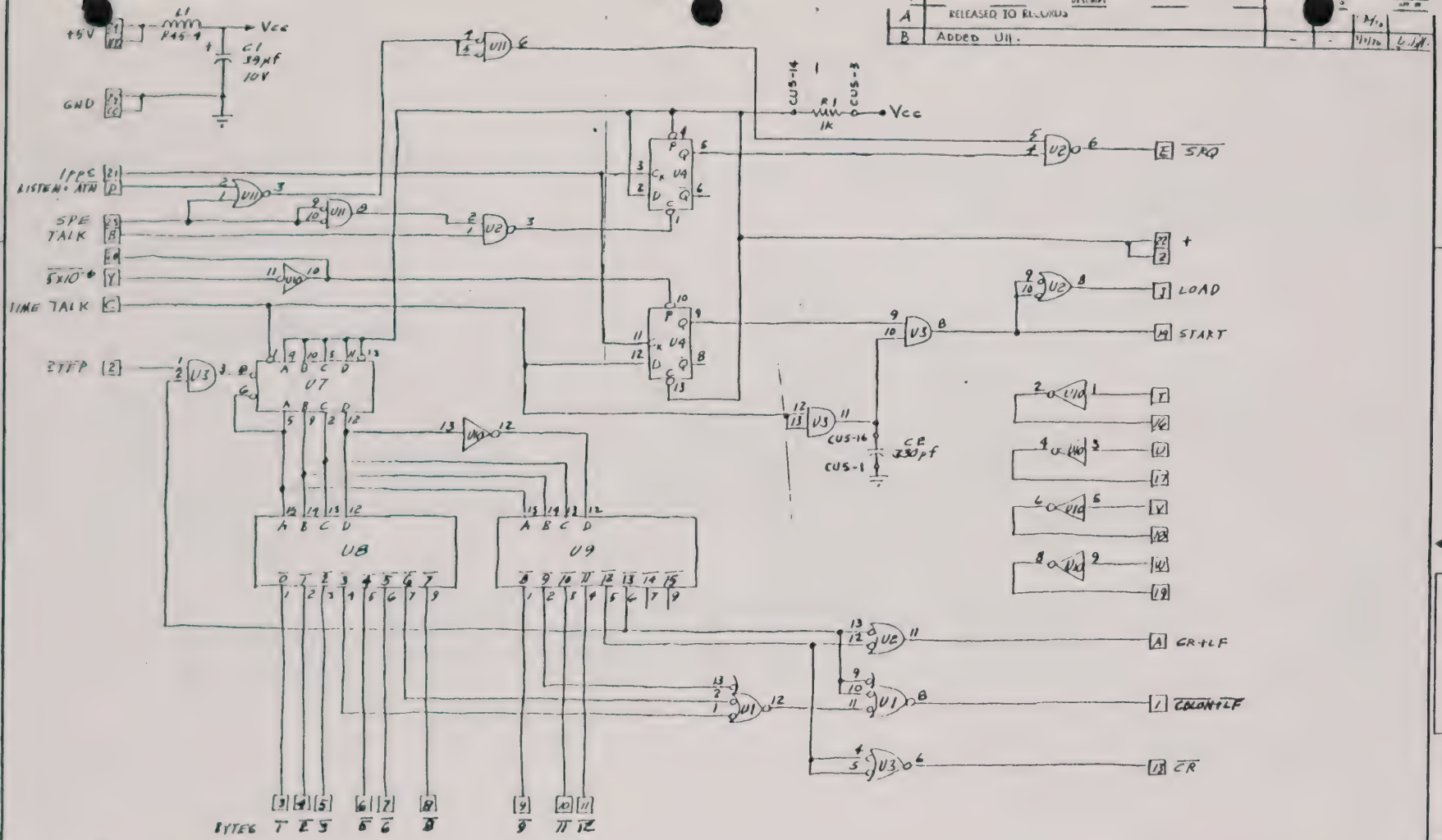
This card develops the $\overline{\text{SRQ}}$, Load and Start signals, generates the character selection signals and inverts the 8-4-2-1 bit signals from the time latches. In addition, it develops signals used to form the colon, carriage return and line feed characters in the time format.

2) CIRCUIT DESCRIPTION

When the time data sequence begins the Talk input to pin C goes high removing the count 15 preset from character counter U7 and initiating a Start via U3-11, U3-8 and pin 14. The Load output from U2-8 goes low freezing the time data in the latch buffer via pin J. The first $\overline{\text{Step}}$ input at pin 2 advances U7 to a count of "0" gating the first character onto the bus via decoder U8 and pin 3. Decoders U8 and U9 convert the binary output from U7 to 16-line. Subsequent $\overline{\text{Step}}$ inputs advance U7 through the sequence of 14 characters. Gates U1-12, U1-8, U2-11 and U3-6 select and form the colon, carriage return and line feed characters. The first four bits of each data word are fed to the Bus Control #1 Card through inverters on U10.

The $\overline{\text{SRQ}}$ output at pin E is generated at the start of each Code frame provided the unit has been designated a Listener on a Serial Poll Enable state exists. It is cleared when the unit is designated a Talker and the Serial Poll is disabled.

REV	DESCRIPTION			DATE	APPROVED
A	RELEASED TO RECORDS				
B	ADDED U11.			9/1/76	



NOTES:
1. Resistor is ¼w, 5%.
2. I C's

U1	SN7411N	(GND - PIN 7 / Vcc - PIN 14)
U2	MC 8616P	(" " " ")
U3	MC1006P	(" " " ")
U4	SN7474N	(" " " ")
U7	SN74S197N	(" " " ")
U8, U9	SN7442AN	(GND-PIN 8/Vcc - PIN 16)
U10	MC 8T26P	(GND-PIN 7/Vcc - PIN 14)
U11	MC 8210P	(" " " ")

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LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

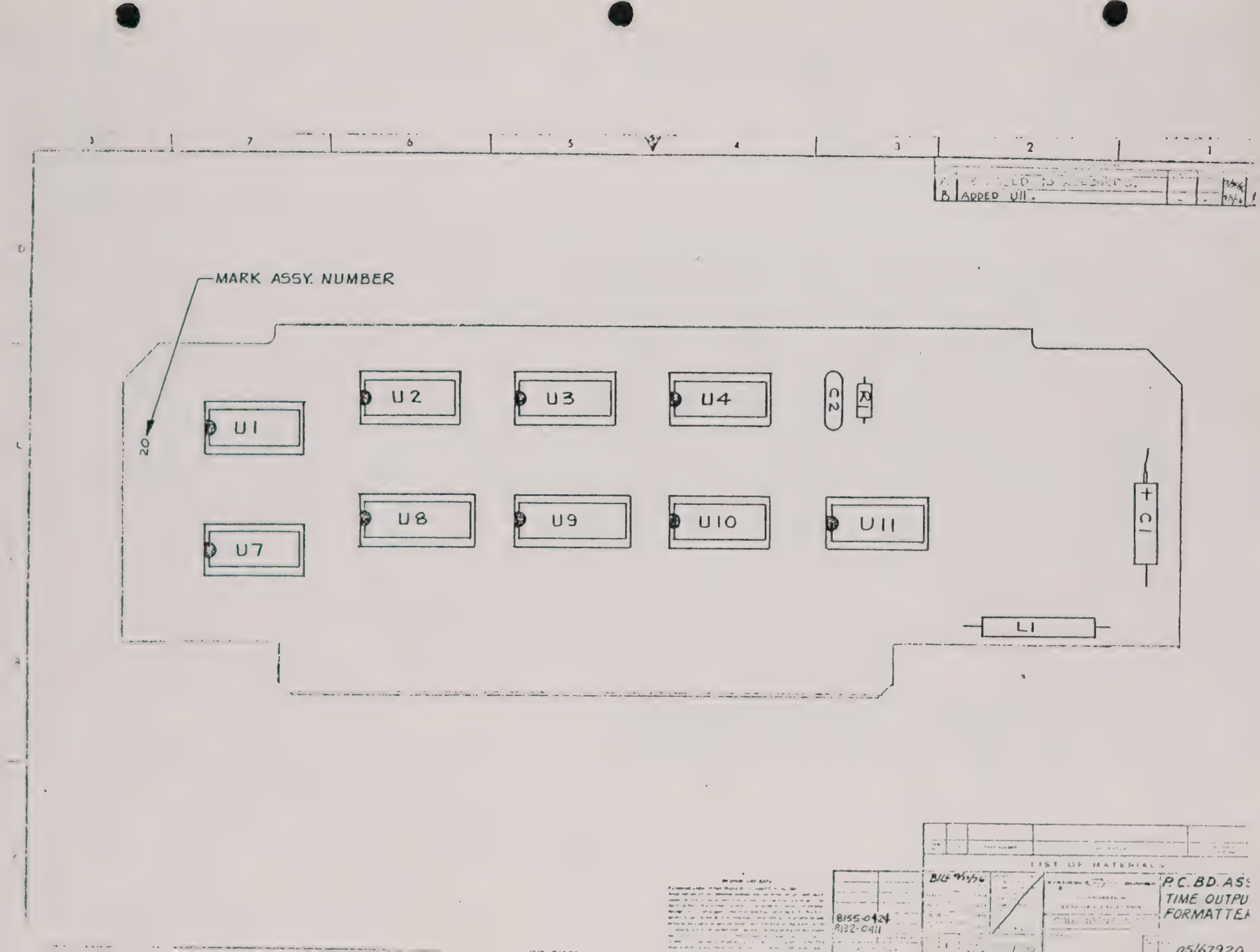
DRAWN	DATE	UNLESS OTHERWISE SPECIFIED / DIMENSIONS ARE IN INCHES / DECIMAL TOLERANCE ± .XX ± .XXX ANGLES ±	BYTRON DONNER CORPORATION CONCORD CALIFORNIA
CHECK	DATE		
ENGR	DATE		
MECH	DATE		
PROJ. ENGR.	DATE		
QA	DATE		
USED ON	NEXT ASSY		
APPLICATION		SCALE / DO NOT SCALE DRAWING	SH 1 OF 1

TIME OUTPUT FORMATTER

CODE IDENT 52947

MATERIAL

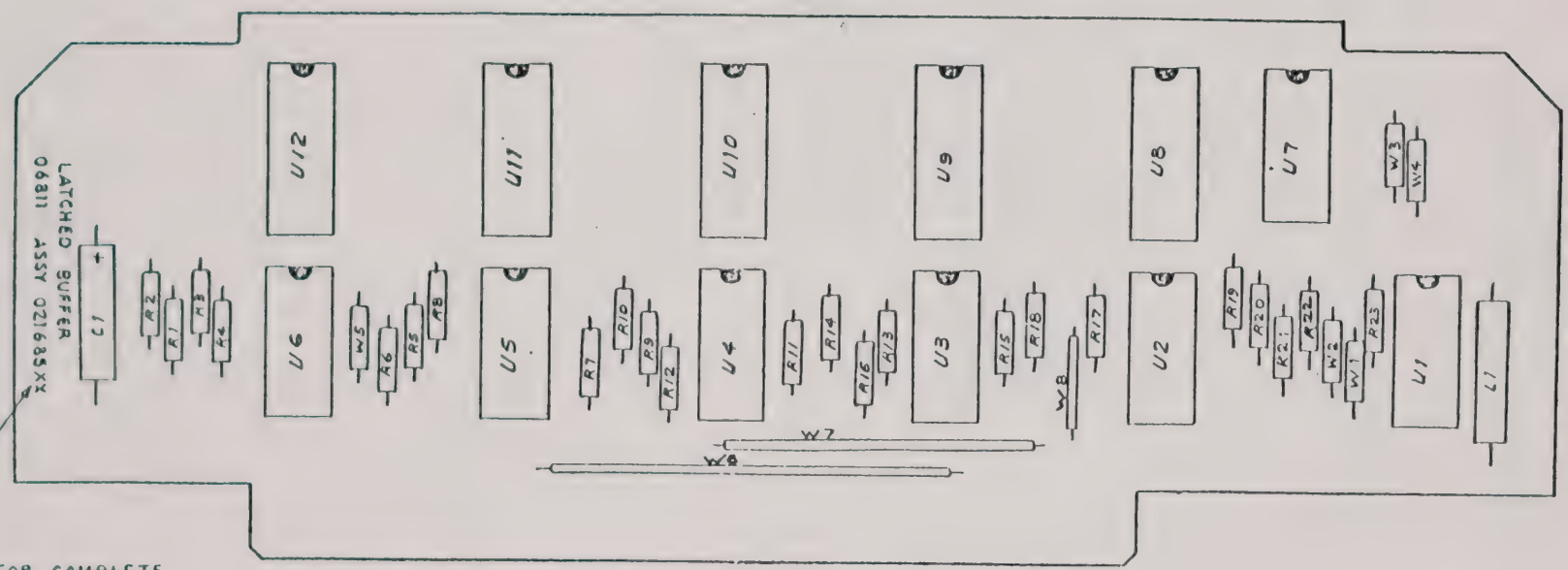
DRAWING NO			
REF	SIZE	PART NO	REV
7	C	051619 20	B


MARK ASSY. NUMBER
20
U1
U2
U3
U4
C2
R1
U7
U8
U9
U10
U11
C1
L1
B ADDED U11.
LIST OF MATERIALS
8155-0424
8132-0411
P.C. BD. ASS
TIME OUTPU
FORMATTE

PARTS LIST
TIME OUTPUT FORMATTER
#05167920 REV B

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	05167920
	Schematic	7-05167920
	Extractor	100865
L1	Inductor, R45-4	101313
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 330 pF	100276
XU1-4,7,10,11	Integrated Circuit Socket, 14 Pin	103349
XU8-9	Integrated Circuit Socket, 16 Pin	103350
U1	Integrated Circuit, SN7411N	025750
U2	Integrated Circuit, MC846P	019716
U3	Integrated Circuit, MC1806P	025733
U4	Integrated Circuit, SN7474N	025241
U7	Integrated Circuit, SN74LS197N	103165
U8-9	Integrated Circuit, SN7442AN	025749
U10	Integrated Circuit, MC836P	025704
U11	Integrated Circuit, MC1810P	025735

REVISIONS			
A.	W6 WAS W8 ; W8 WAS W6.	—	



— MARK FOR COMPLETE ASSY. NUMBER.

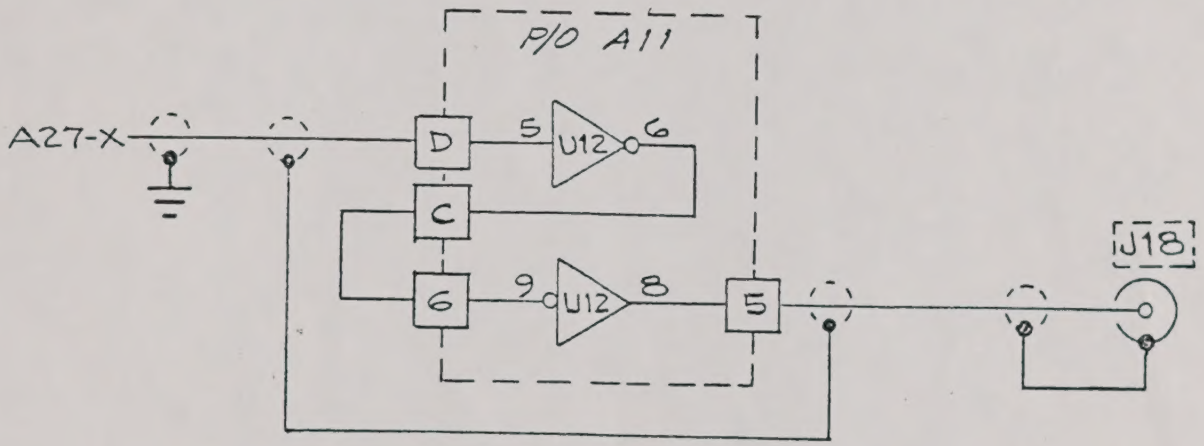
							LATCHED BUFFER
							021685D01 A

PARTS LIST

LATCHED BUFFER #7-02168502

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #02168501)	02168502
	Schematic	7-02168502
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
R1-20	Not Used	
R21	Resistor, 1 k 5%, 1/4 W	101569
R22-23	Resistor, 10 k 5%, 1/4 W	101570
U1	Integrated Circuit, MC857P	025753
U2-6	Integrated Circuit, MC1808P	025734
U7	Integrated Circuit, SN7404N	025779
U8-12	Integrated Circuit, SN74L75N	045201
W1	Not Used	
W2	Jumper, Molded	102879
W3	Not Used	
W4	Jumper, Molded	102879
W5	Not Used	
W6-8	Jumper, Insulated	
	Extractor	100865

REVISIONS					
ISSUE	DESCRIPTION	SAR NO.	ECO NO.	DATE	APP BY
A	RELEASE TO RECORDS	—	—	[illegible]	KR



NOTES:
1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON THE BASIC UNIT BLOCK DIAGRAM #7-06102806.

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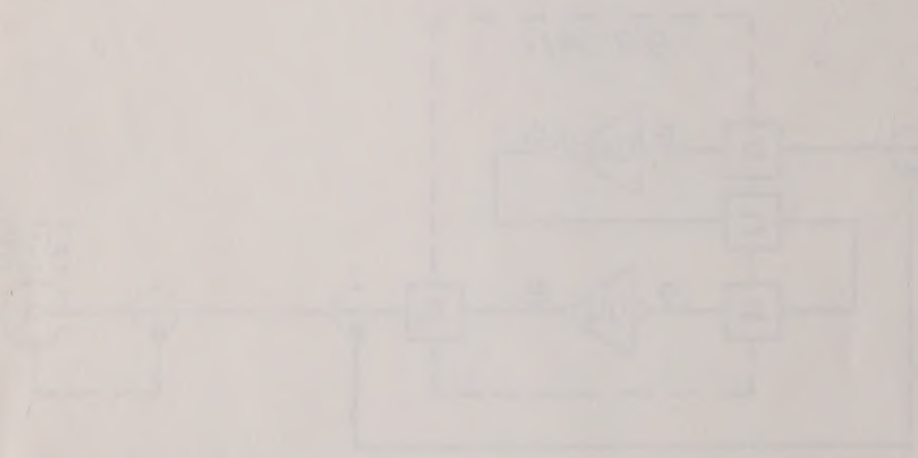
		DRAWN [illegible] DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.03 .XXX ±.010 ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	1 MHZ BUFFERED OUTPUT
		CHECK DATE			
		ELECT DATE			
		MECH DATE			
		PROJECT [illegible]		CODE IDENT. 52542	
2152-10 11057		Q.A. DATE			
USED ON	NEXT ASSY	SCALE — DO NOT SCALE DRAWING	DWG SIZE A	MATERIAL	REF 7
APPLICATION			SH 1 OF 1		DWG NO. 07187603 ISSUE A